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B-TC-6300QB-0-DBU	6300QB MICRO VAX III WORLD BOX (TC)
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B-DD-6300QB-0-DBU	6300QB MICRO VAX III WORLD BOX (DD ONLY)
B-CD-M7606-0-0	MICRO VAX III CPU (DD ONLY)
D-UA-M7606-0-0	MICRO VAX III CPU
K-PL-M7606-0-DBP	MICRO VAX III CPU (PL)
D-CS-M7606-0-1	MICRO VAX III CPU
B-DD-5416744-0-0	FUNCTION SEL/SLU CONSOLE CONN (DD ONLY)
D-UA-5416744-0-0	FUNCTION SEL/SLU CONSOLE CONN
K-PL-5416744-0-DBP	FUNCTION SEL/SLU CONSOLE CONN (PL)
D-CS-5416744-0-1	FUNCTION SEL/SLU CONSOLE CONN
B-DD-M9047-0-0	Q BUS GRANT CONTINUITY CARD (DD ONLY)
D-UA-M9047-0-0	Q BUS GRANT CONTINUITY CARD
D-CS-M9047-0-1	Q BUS GRANT CONTINUITY CARD
A-PS-1700712-0-0	CABLE ASSY, 20 PIN
A-PS-1700624-0-0	CABLE CONSOLE BACKPLANE
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A-PS-1700301-0-0	CABLE ASSY, 7 COND
MP-02049-01	PRINT SET BA123-A BASIC ENCLOSURE

UNIT VARIATIONS
COVERED BY THIS
PRINT SET

630QB
FIELD MAINTENANCE
PRINT SET

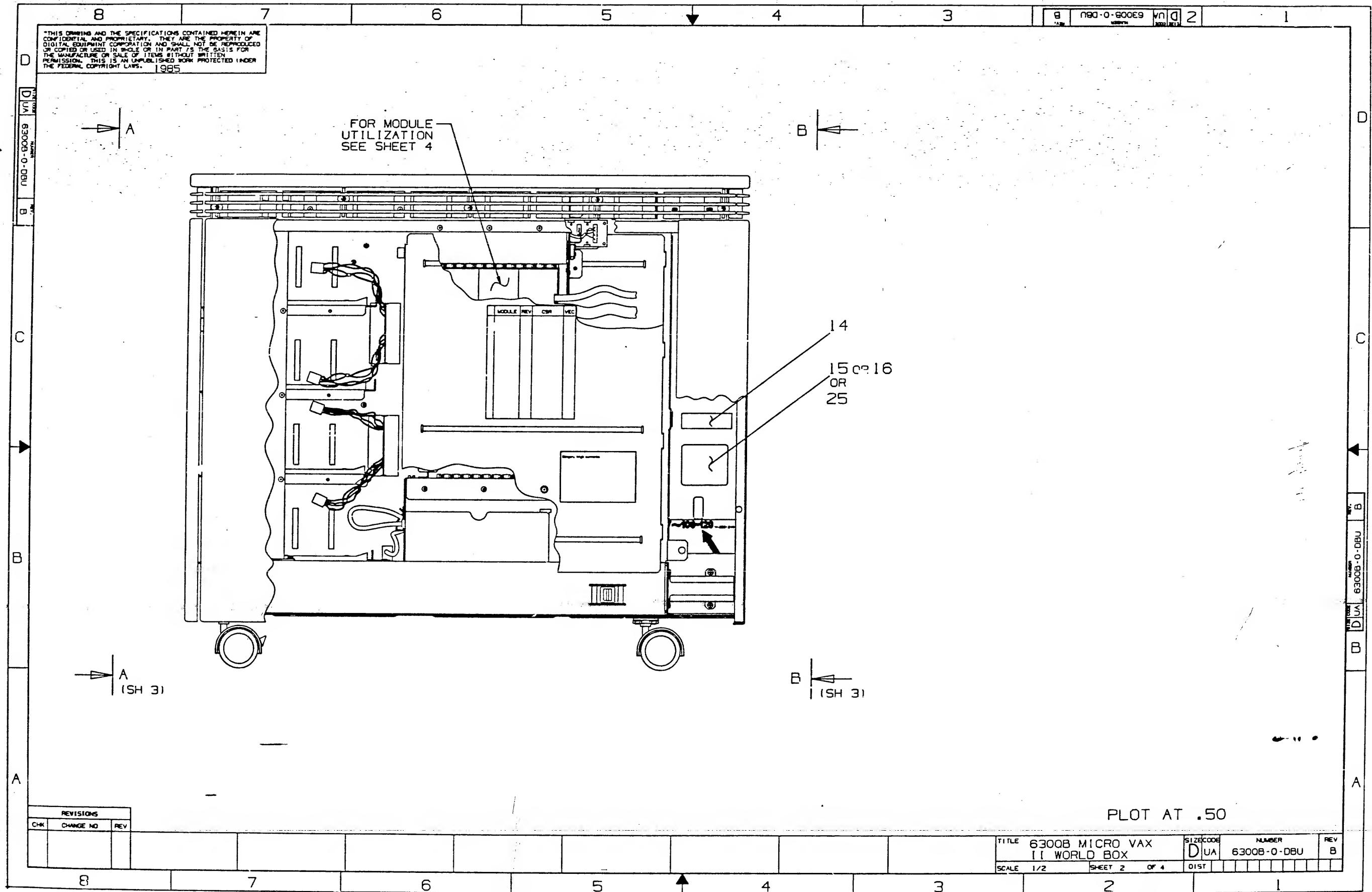
DIGITAL EQUIPMENT CORPORATION

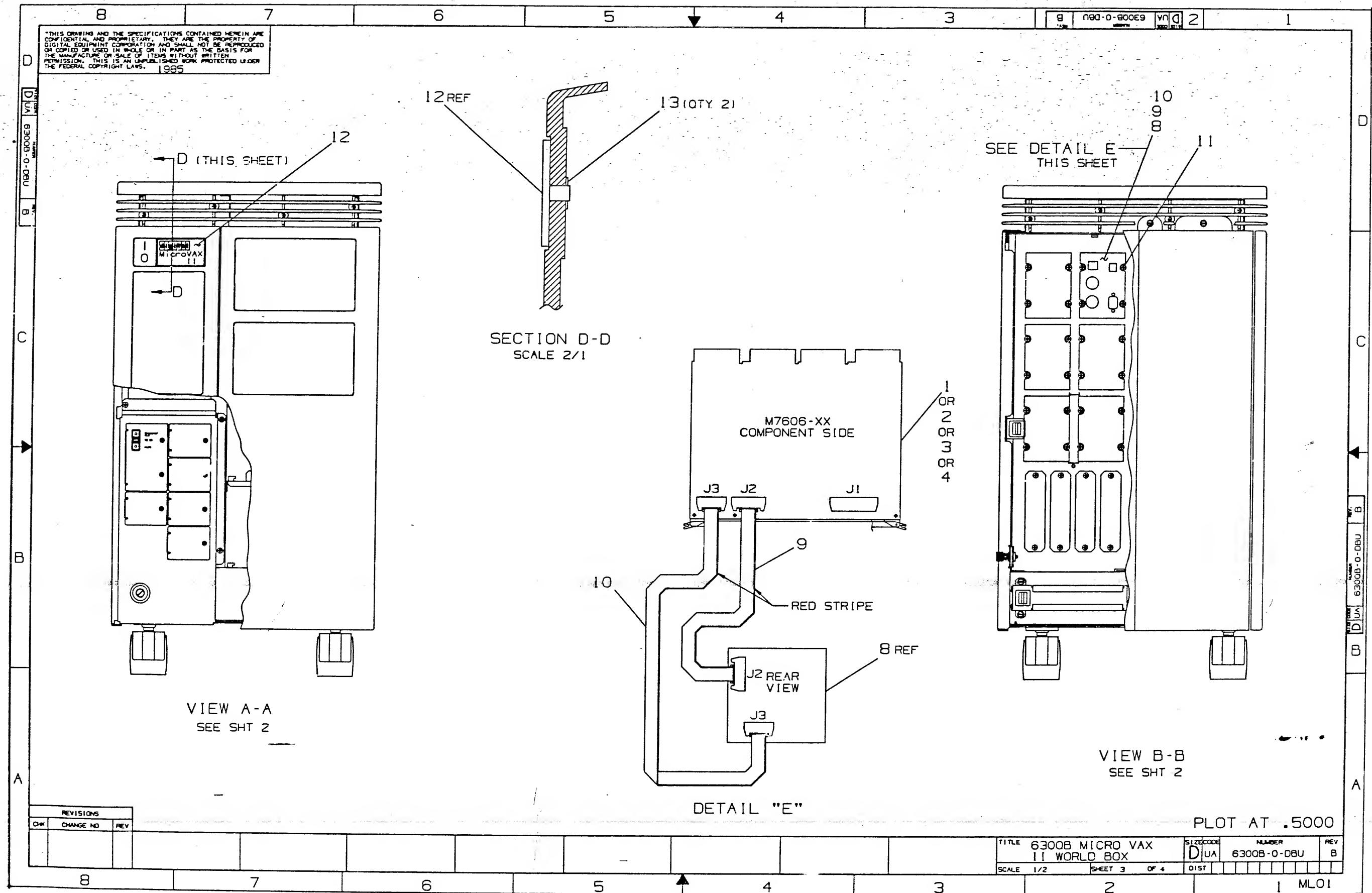
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NUMBER MP-02071-01
REV A1

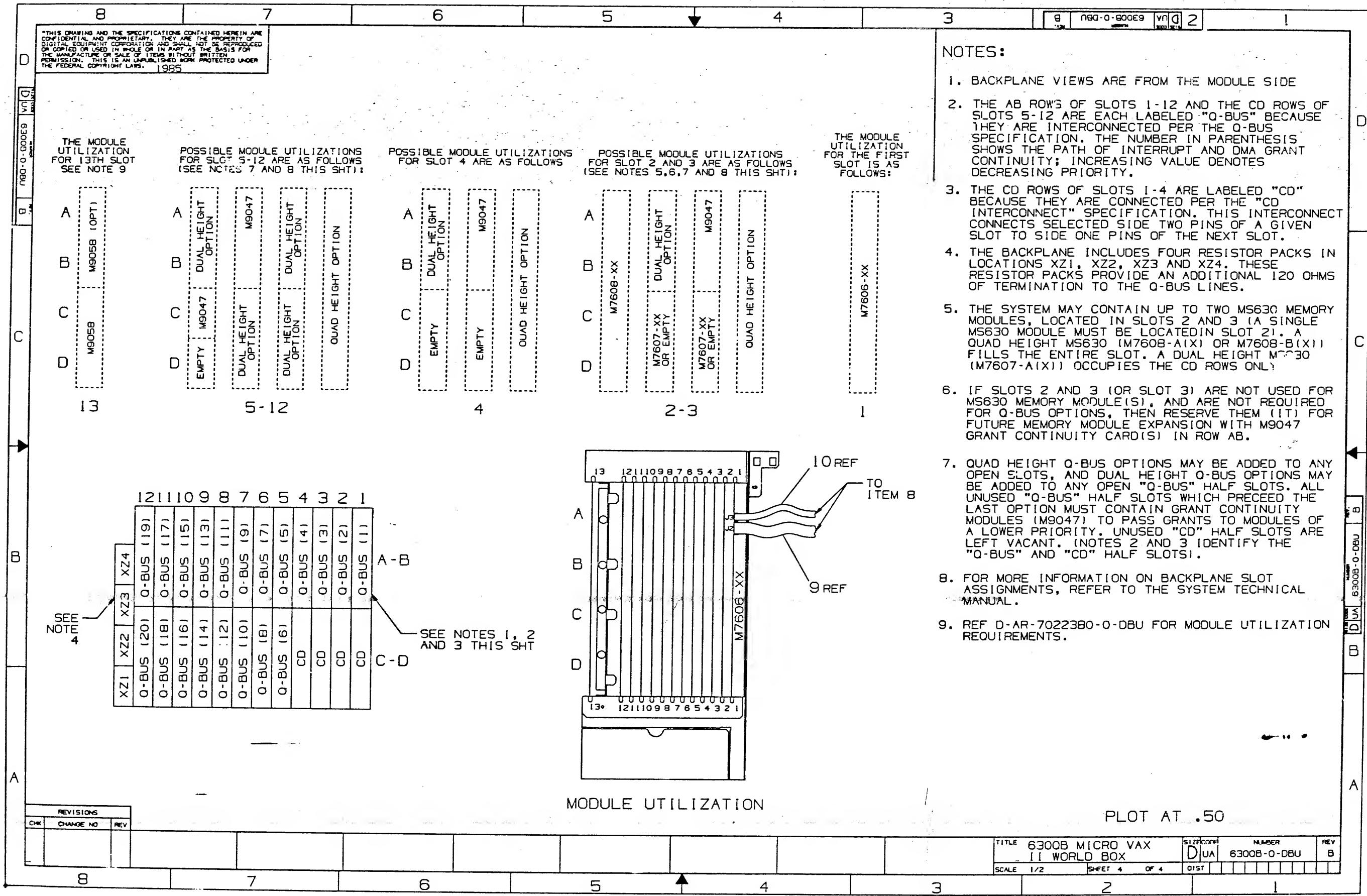
FILE NAME: TC-630QB-O-DBUA

REVISION HISTORY		REV.		
DATE	ECO NUMBER	INITIAL		
			DRN. D. HEALY	DATE 25FEB85
			CHK'D D. HEALY	DATE 19MAR85
			DES. ENG. J. NICHOLS	DATE 19MAR85
			RESP. ENG. K. WORTMAN	DATE 19MAR85
			FIELD SERVICE	DATE
TOP DOC. B-DD-630QB-0-DBU				
		TITLE		digital
		630QB MICRO VAX II WORLD BOX		
		SIZE CODE	NUMBER	REV.
		B TC	630QB-0-DBU	A
				SHEET 1 OF 1

MLO 1







LINE ITEM	TOP DOCUMENT	PART NUMBER	REV	DESCRIPTION	VARIATION	REVISION LEVEL:	QTY PER VARIATION						
							A2	A3	B2	B3	C2	C3	D2
A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2
1	1	B-DD-M7606-0-0	M7606-AA	MICROVAX II W/1MB,FP, INCLUDES TI			1	1	-	-	-	-	-
2	2	B-DD-M7606-0-0	M7606-BA	M7606-AA W/NO FP (CPU,1MB) = M76			-	-	1	1	-	-	-
3	3	B-DD-M7606-0-0	M7606-CA	M7606-AA W/256KB MEM (CPU,256KB,			-	-	-	1	1	-	-
4	4	B-DD-M7606-0-0	M7606-DA	M7606-AA W/256KB MEM, NO FP = M76			-	-	-	-	1	1	
5	5	K-PL-7022382-0-DBP	7022382-02	BA123-A ACCESSORY KIT			1	1	1	1	1	1	1
6	6	B-DD-7022380-0-DBU	7022380-01	BA123-A BASIC ENCLOSURE (120V)			-1	-	1	1	-	1	-
7	7	B-DD-7022380-0-DBU	7022380-02	BA123-A BASIC ENCLOSURE (240V)			-	1	-	1	-	1	-
8	8	B-DD-5416744-0-0	5416744-01	FUNCTION SEL/SLU CONSOLE CONNECT			1	1	1	1	1	1	1
9	9	A-PS-1700712-0-0	1700712-02	A WIRE HARN ASSY 20COND 30AWG 20SK			1	1	1	1	1	1	1
10	10	A-PS-1700624-0-0	1700624-01	A CABLE ASSY, 10COND, FLAT, 10(2X05)I			1	1	1	1	1	1	1
11	11	A-PS-9010174-0-0	9010174-00	C SCREW, SEMS PAN PHIL 6-			4	4	4	4	4	4	4
12	12	D-MD-7431480-0-0	7431480-03	A MEDALLIAN SYSTEM LOGO (630QB)			1	1	1	1	1	1	1
13	13	A-PS-9009257-0-0	9009257-02	D RING, RETAINER EXTERNAL FOR .188			2	2	2	2	2	2	2
14	14	A-PS-3617880-0-0	3617880-02	LABEL, FCC, CLASS A, PROCESSOR			1	1	1	1	1	1	1
15	15	A-PS-3624471-0-0	3624471-01	A LABEL, BUSINESS COMP BA123-A2			1	-	1	-	1	-	1
16	16	A-PS-3624471-0-0	3624471-02	A LABEL, BUSINESS COMP BA123-A3			-	1	-	1	-	1	-
17	17	A-PS-1700198-0-0	1700198-00	B PWR CORD, TERM 3-18		250	-	REF	-	REF	-	REF	-
18	18	A-PS-1700199-0-0	1700199-00	A PWR CORD, TERM 3		250	-	REF	-	REF	-	REF	-
19	19	A-PS-1700209-0-0	1700209-00	A PWR CORD, TERM 3-.75MM 5A		250	-	REF	-	REF	-	REF	-
20	20	A-PS-1700210-0-0	1700210-01	A PWR CORD, TERM 3-.75MM 250V 6		250	-	REF	-	REF	-	REF	-
21	21	A-PS-1700310-0-0	1700310-01	A PWR CORD, TERM 3-.75MM		250	-	REF	-	REF	-	REF	-
22	22	A-PS-1700364-0-0	1700364-01	A PWR CORD, TERM 3-.75MM		250V	-	REF	-	REF	-	REF	-
23	23	D-AR-7022380-0-DBU		BA123-A SYSTEM ARRANGEMENT			REF	REF	REF	REF	REF	REF	REF
24	24	B-DD-M9047-0-0	M9047-00	QBUS GRANT CONTINUITY, 1ST USED I			A/R	A/R	A/R	A/R	A/R	A/R	A/R
25	25	A-PS-3617674-0-0	3617674-22	LABEL, SERIAL/POWER, W/UL & CSA MA			A/R	A/R	A/R	A/R	A/R	A/R	A/R

REVISION HISTORY			BASIC PART NO: 630QB		DRN: D. RICHARD		DATE: 19-FEB-85		D I G I T A L				
ENG	ECO NUMBER	REV	SECTION A OF A		CHK'D:	D. HEALY	DATE:	19-MAR-85	TITLE PARTS LIST				
JN	630QB-ML001	B	SECTION VARIATION INDEX		[A]A2,A3,B2,B3,C2,C3, D2,D3	[B]	DES.ENG:	J. NICHOLS	630QB MICRO VAX II WORLD BOX				
			[C]				RESP.ENG.:	J. NICHOLS	DOCUMENT NUMBER				
			[D]				DATE:	19-MAR-85	SIZE	CODE	NUMBER	! REV	
			[E]				MFG.ENG.:	K. WORTMAN	K PL 630QB-0-DBP				
			[F]				ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	RELEASE DATE: 07-MAY-85				
			D-UA-630QB-0-DBU				!B-DD-630QB-0-DBU	!FILE NAME: ML863B.PLS	EDIT # 14				

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LINE ITEM TOP DOCUMENT

MIN
PART NUMBER REV DESCRIPTIONQTY PER VARIATION
VARIATION REVISION LEVEL: A2 A3 B2 B3 C2 C3 D2 D3

26 NOTE: DEPENDING ON RAM VENDOR, MODULE MAY BE STAMPED AD/AH, BC/BH, CC/CH, DC/DH

TITLE		SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
D I G I T A L	630QB MICRO VAX II WORLD BOX		K	PL	630QB-0-DBP	B

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DRAWING DIRECTORY

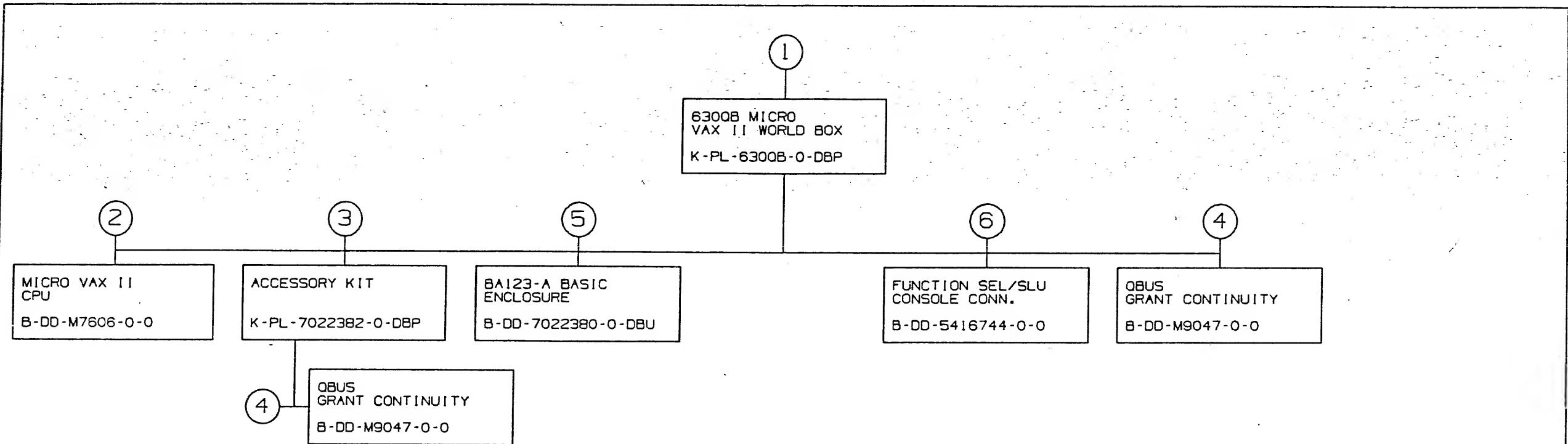
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UNIT VARIATIONS

FILE NAME: DD-630QB-O-DBUA

REVISIONS	CHANGE NO.	REV.	INITIAL A	USED ON OPTION/MODEL	DRN.	DATE	TITLE	digitel	
					D. HEALY	25FEB85	CHK'D	DATE	6300B MICRO VAX
					D. HEALY	19MAR85	PROJ. ENG.	DATE	I I WORLD BOX
					J. NICHOLS	19MAR85	PROD.	DATE	
					K. WORTMAN	19MAR85			
					TOP DOC.				
					B-DO-6300B-0-DBU				
					SHEET 1 OF 3		DIST.		
	CHK								

MLQ 1



TITLE: 630QB MICRO VAX
II WORLD BOX

SHEET 2 OF 3

SIZE CODE
B DD

NUMBER
630QB-0-DBU

REV.
A

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS								SIZE CODE	CODE			
				B1	C1	D1	E1	F1	H2	H2						
		M7606	KA630													
D-UA-M7606-0-0	1		KA630 UNIT ASSEMBLY	A	A	B	B	B	B	B						
K-PL-M7606-0-DBP	2		KA630 PARTS LIST	A	B	C	D	E	F	H						
K-PC-M7606-0-DBJ	1		P.C. DESIGN DATA BASE	E	E	E	E	E	E	E						
		5016523-01	ETCHED CIRCUIT BOARD	E1	E1	E1	E1	E1	E1	E1						
B-DD-5016523-0-0	1		DRAWING DIRECTORY	A	A	A	A	A	A	A						
B-CS-M7606-0-1	1		M7606 DRAWING DIRECTORY	-	B	B	B	B	B	B						
B-CS-M7606-0-2	1		MICROVAX II SYSTEM	-	B	B	B	B	B	B						
B-CS-M7606-0-3	1		KA630-UVAX ON Q22 BUS	-	B	B	B	B	B	B						
B-CS-M7606-0-4	1		UVAX & FPU	-	B	B	B	B	B	B						
D-CS-M7606-0-5	1		UVAX & FPU PINOUTS	-	-	-	-		A	A						
B-CS-M7606-0-6	1		ADDRESS LATCH/LOCAL MEMORY DECODE	-	B	B	B	B	B	B						
B-CS-M7606-0-7	1		MEMORY SUBSYSTEM	-	B	B	B	B	B	B						
B-CS-M7606-0-8	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B						
B-CS-M7606-0-9	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B						
B-CS-M7606-0-10	1		DC380 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY	-	B	B	B	B	B	B						
B-CS-M7606-0-11	1		REFRESH LOGIC/COUNTER	-	B	B	B	B	B	B						
B-CS-M7606-0-12	1		DIVIDE BY 12	-	B	B	B	B	B	B						
B-CS-M7606-0-13	1		SYNCHRONOUS 3 BIT COUNTER	-	B	B	B	B	B	B						
NOTES:				REVISION HISTORY	DATE	ECO NO.	REV.	A	B	C	D	E	F	H		
NOTE: MODULE PART REV H' WAS USED FOR VAXSTATION FIELD UPGRADE KIT ONLY. M7606 ECO-00006 REWORKED VARIATION M7606 AH TO EITHER M7606-2 (NEW NEC) M7606-ZP (MITSUBISHI) M7606 OR M7606-ZF (HITACHI). THERE WAS NO PART REV CHANGE.								5/84	INIT	5/85	ML001	6/85	ML002	7/85		
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								DOCUMENT NUMBER								
				SHEET 1 OF 4												

DRAWING NO.	NO OF SHTS.	PART NO.	DESCRIPTION	REVISIONS													
				SIZE	CODE	B	D	D	H	REV.	M7606-0-0	NUMBER	REV.				
B-CS-M7606-0-14	1		VECTOR HACK	-		B	B	B	B	B							
B-CS-M7606-0-15	1		INVERTING MUX LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-16	1		4 to 1 MUX	-		B	B	B	B	B							
B-CS-M7606-0-17	1		Q-BUS SUPPORT LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-18	1		BLK MD CTR LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-19	1		TOGGLE FLOP	-		B	B	B	B	B							
B-CS-M7606-0-20	1		Q-BUS SUPPORT LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-21	1		Q-BUS SUPPORT LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-22	1		Q-BUS SUPPORT LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-23	1		Q-BUS SUPPORT LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-24	1		POWER BUFFER MACRO	-		B	B	B	B	B							
B-CS-M7606-0-25	1		BIDIRECT BUFFER	-		B	B	B	B	B							
B-CS-M7606-0-26	1		MUX LOGIC	-		B	B	B	B	B							
B-CS-M7606-0-27	1		TRANSLATION MAP GROUP	-		B	B	B	B	B							
B-CS-M7606-0-28	1		KA630 Q-BUS INTERFACE	-		B	B	B	B	B							
B-CS-M7606-0-29	1		UVAX INTERFACE GATE ARRAY	-		B	B	B	B	B							
B-CS-M7606-0-30	1		DC379 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRIP ARRAY	-		B	B	B	B	B							
B-CS-M7606-0-31	1		UVAX INTERFACE GATE ARRAY DATA PATH	-		B	B	B	B	B							
B-CS-M7606-0-32	1		UVDAL I/O BUFFERS, ADDR LATCHES	-		B	B	B	B	B							

NOTES:

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1984



REVISION HISTORY

DATE ECO NO. REV.

5/84 INIT

5/85 ML001

6/85 ML002

7/85 ML003

8/85

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ML005

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DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS							
				-	B	B	B	B	B	B	B
B-CS-M7606-0-33	1		ADDRESS DECODER	-	B	B	B	B	B	B	
L-CS-M7606-0-34	1		EXCEPTIONS AND INTERRUPTS	-	B	B	B	B	B	B	
B-CS-M7606-0-35	1		UVAX INPUTS AND I/O PINS	-	B	B	B	B	B	B	
B-CS-M7606-0-36	1		BOOT/DIAG REG., MEM ERR ADDR REG.	-	B	B	B	B	B	B	
B-CS-M7606-0-37	1		EPR BUS, X DAL BUS	-	B	B	B	B	B	B	
B-CS-M7606-0-38	1		INTERNAL DATA BUSES	-	B	B	B	B	B	B	
B-CS-M7606-0-39	1		MISC. CONTROL STROBES	-	B	B	B	B	B	B	
B-CS-M7606-0-40	1		RESET COUNTER, POWER UP/DOWN CNTRL	-	B	B	B	B	B	B	
B-CS-M7606-0-41	1		MEMORY SYSTEM ERROR REGISTER	-	B	B	B	B	B	B	
B-CS-M7606-0-42	1		TIME OF YEAR (TOY) CLOCK	-	B	B	B	B	B	B	
B-CS-M7606-0-43	1		CONSOLE SERIAL LINE INTERFACE	-	B	B	B	B	B	B	
B-CS-M7606-0-44	1		LEDS AND CONFIGURATION CONNECTOR	-	B	B	B	B	B	B	
B-CS-M7606-0-45	1		DECOUPLING CAPACITORS	-	B	B	B	B	B	B	
B-CS-M7606-0-46	1		KA630 STATE MACHINES	-	B	B	B	B	B	B	
B-CS-M7606-0-47	1		UVAX CYCLE CONTROLLER	-	B	B	B	B	B	B	
B-CS-M7606-0-48	1		MEMORY SEQUENCER	-	B	B	B	B	B	B	
B-CS-M7606-0-49	1		MEMORY SEQUENCER SUPPORT	-	B	B	B	B	B	B	
B-CS-M7606-0-50	1		Q22 BUS STATE MACHINES	-	B	B	B	B	B	B	
D-CS-M7606-0-51	1		KA630 MEMORY ARBITER LISTING	-	-	-	-	-	A	A	

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digital

DRB 128C
EN-01242-16-REVA(396)

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS									
B-CS-M7606-0-52	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B			
B-CS-M7606-0-53	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B			
D-CS-M7606-0-54	1		KA630 LOCAL I/O CONTROL MACHINE	-	-	-	-	-	A	A			
			UL TESTING	-	-	-	-	-					
B-CS-M7606-0-55	1		KA630 LOCAL I/O BUS CONTROL	-	B	B	B	B	B	B			
D-CS-M7606-0-56	1		KA630 Q-BUS ARBITRATION CONTROL MACHINE LISTING	-	-	-	-	-	A	A			
B-CS-M7606-0-57	1		Q-BUS ARBITRATION CONTROLLER DETAILED CONTROL FLOW DIAGRAM	-	B	B	B	B	B	B			
D-CS-M7606-0-58	1		Q22 BUS MASTER CONTROL MACHINE LISTING	-	-	-	-	-	A	A			
B-CS-M7606-0-59	1		Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B			
D-CS-M7606-0-60	1		Q22 BUS SLAVE CONTROL MACHINE LISTING	-	-	-	-	-	A	A			
B-CS-M7606-0-61	1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B			
B-CS-M7606-0-62	1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B			
D-CS-M7606-0-63	1		IKKL RAS DECODE FROM (ETS) LISTING	-	-	-	-	-	A	A			
D-CS-M7606-0-64	1		PALASM LISTING FOR PALISLSA DEVICES	-	-	-	-	-	A	A			
D-CS-M7606-0-65	1		MNEMONIC DICTIONARY	-	-	-	-	-	A	A			
K-DO-M7606-0-0	24		M7606 CROSS REF LIST	-	A	A	A	A	A	A			
NOTES:													
				REVISION HISTORY									
				DATE	ECO NO.	REV.	A	B	C	D	E	F	H
				5/84	INIT								
				5/85	ML001								
				6/85	ML002								
				7/85	ML003	D							
				8/85	ML004								
				1/86	ML005								
				3/86	ML006								
										DRN. D.DROZD DATE 5/17/84	TITLE KA630		
										CHK'D E.LANDRY DATE 5/17/84	DOCUMENT NUMBER		
										DES. ENG. B.MASKAS DATE 5/17/84			
										RESP. ENG. B.MASKAS DATE 5/17/84	SIZE B	CODE DD	NUMBER M7606-0-0
										MFG. ENG. B.SCHULTE DATE 9/24/84	REV. H		SHEET 4 OF 4

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1984

digital

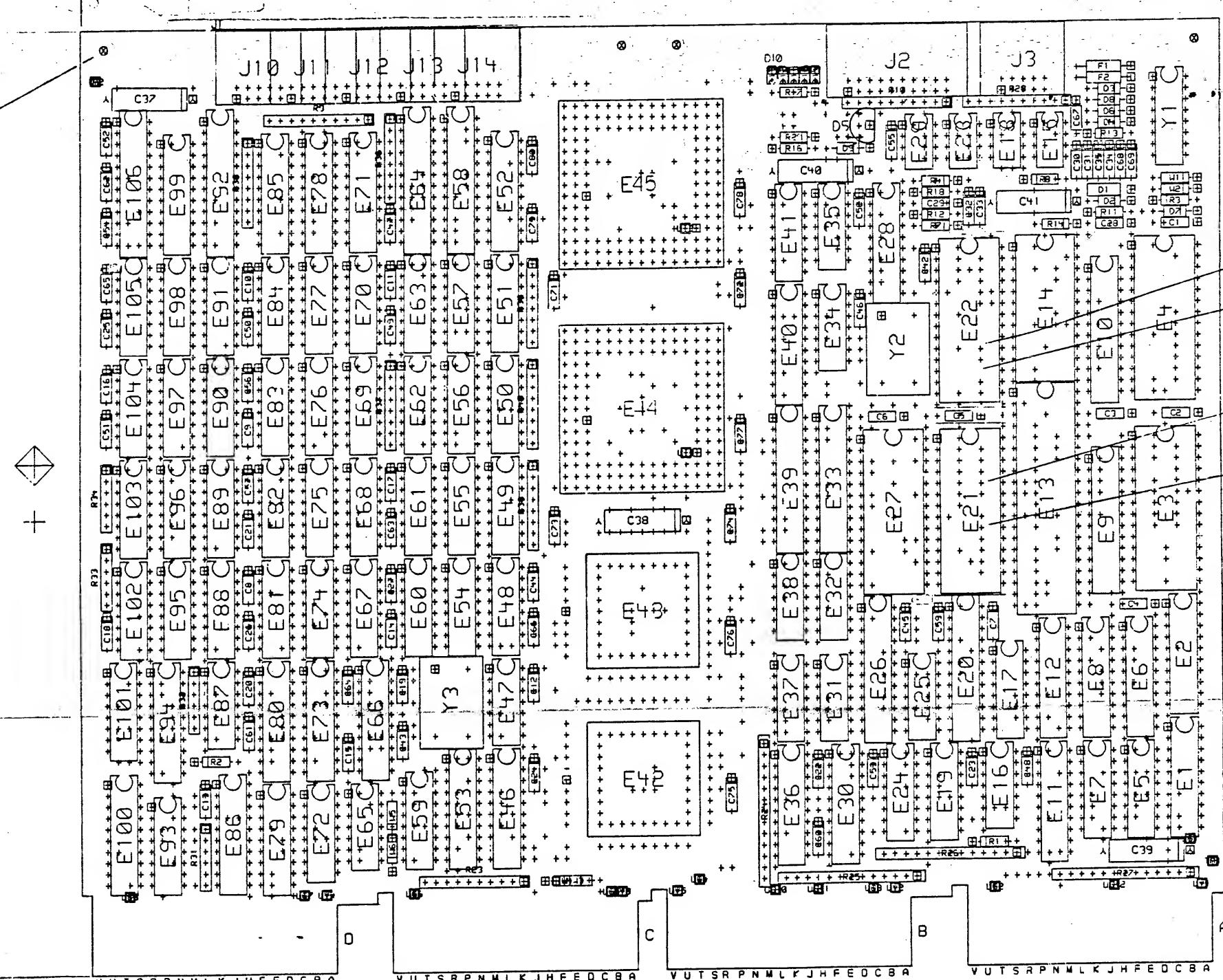
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REWORK INSTRUCTIONS

1. COMPONENT DELETES
2-1 DELETE E21 P/N 23035E6-00
2-2 DELETE E22 P/N 23034E6-00

2. COMPONENT ADDS.
2-3 DELETE E21 P/N 23063E6-00
2-4 DELETE E22 P/N 23062E6-00

(QT)



NOTES: 1. NOT INSTALLED

		SIGNATURES	DATE	digital		
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CHK'D.			E-71A			
MECH. ENG.						
PROJ. ENG. FILE N.			10-15			
PROD. MFG. W. SCAFF. D.						
SCALE				SIZE CODE	NUMBER	REV.
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NEXT HIGHER ASSY.						

STEP E ↑ Y AXIS **STEP** ____ **TIMES**
REPEAT → X AXIS **STEP** ____ **TIMES**

8

KA630-AA,-AB,-AC,-AD (M7606) DRAWING DIRECTORY

DATA PATH

- 0 MICROVAX II SYSTEM
- 1 KA630 - uVAX on Q22 Bus
 - 1.1 uVAX & FPU
 - 1.1.1 uVAX & FPU PINOUTS
 - 1.2 ADDRESS LATCH/LOCAL MEMORY DECODE
 - 1.3 Memory Subsystem
 - 1.4 Q22 Bus Interface Gate Array
 - 1.4.1-1.4.2, 1.4.1.1-1.4.1.9
 - 1.5 Translation Map Group
 - 1.6 KA630 QBLUS INTERFACE
 - 1.7 uVAX Interface Gate Array
 - 1.7.1-1.7.2, 1.7.2.1-1.7.2.10
 - 1.8 TOY CLOCK
 - 1.9 Console Serial Line Interface
 - 1.10 LEDS and Configuration Connector
 - 1.11 Decoupling Capacitors

CONTROL

- 2 KA630 State Machines
 - 2.1 uVAX Cycle Controller
 - 2.1.1 MEMORY SEQUENCER
 - 2.1.2 MEMORY SEQUENCER SUPPORT
 - 2.2 Q22 BUS STATE MACHINES

MISC.

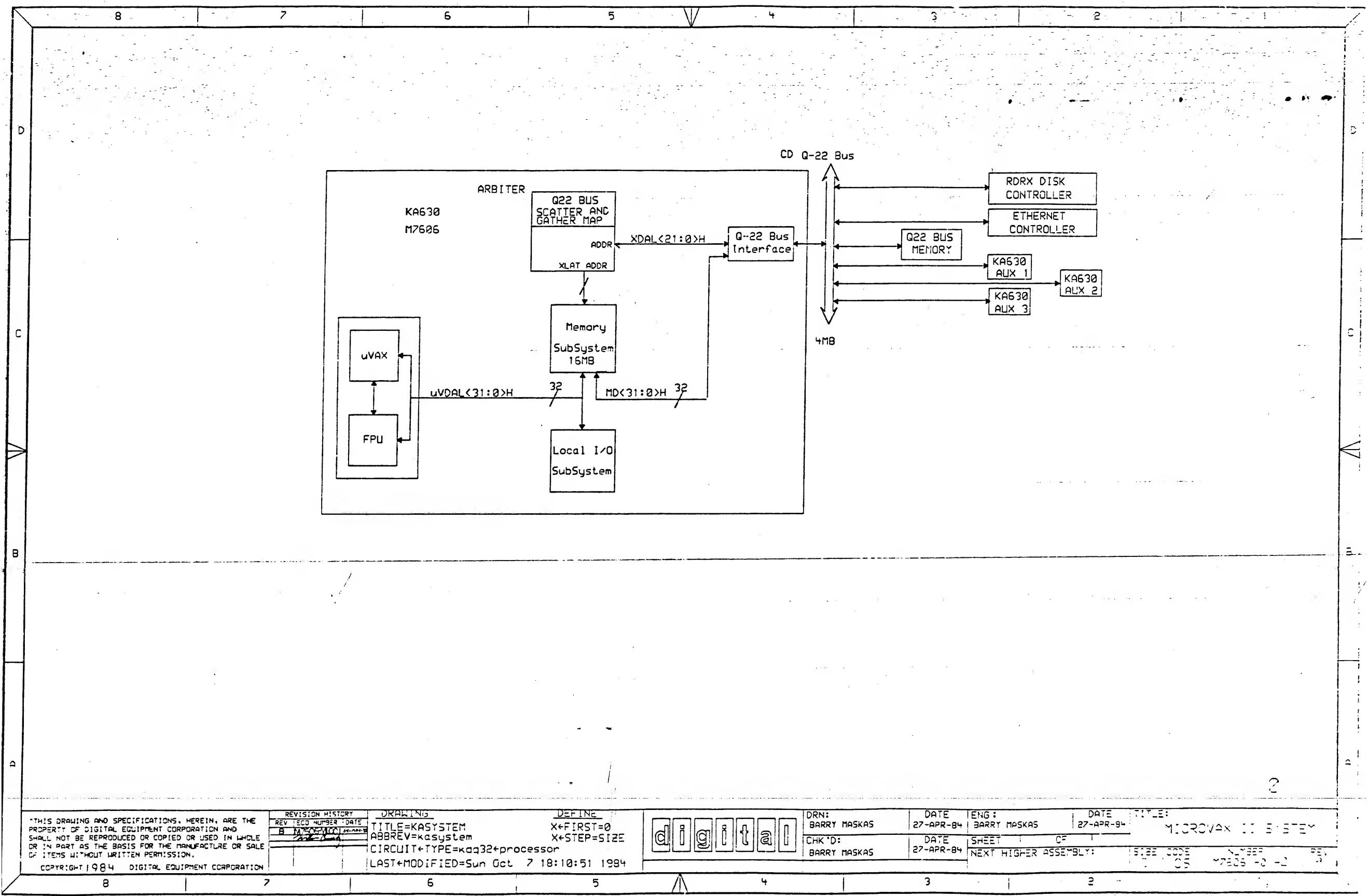
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- 3.1-3.2 KA630 MEMORY ARBITER FLOW DIAGRAM
- 4 KA630 LOCAL I/O CONTROL MACHINE LISTING
- 4.1 KA630 LOCAL I/O CONTROL MACHINE FLOW DIAGRAM
- 5 Q22 BUS ARBITRATION CONTROL MACHINE LISTING
- 5.1 Q22 BUS ARBITRATION CONTROL MACHINE FLOW DIAGRAM
- 6 Q22 BUS MASTER CONTROL MACHINE LISTING
- 6.1 Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM
- 7 Q22 BUS SLAVE CONTROL MACHINE LISTING
- 7.1-7.2 Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM
- 8 1KX4 RAS DECODE PROM (E79) LISTING
- 9 PALASM LISTINGS FOR PAL16L08A DEVICES
- 10 MNEMONIC DICTIONARY

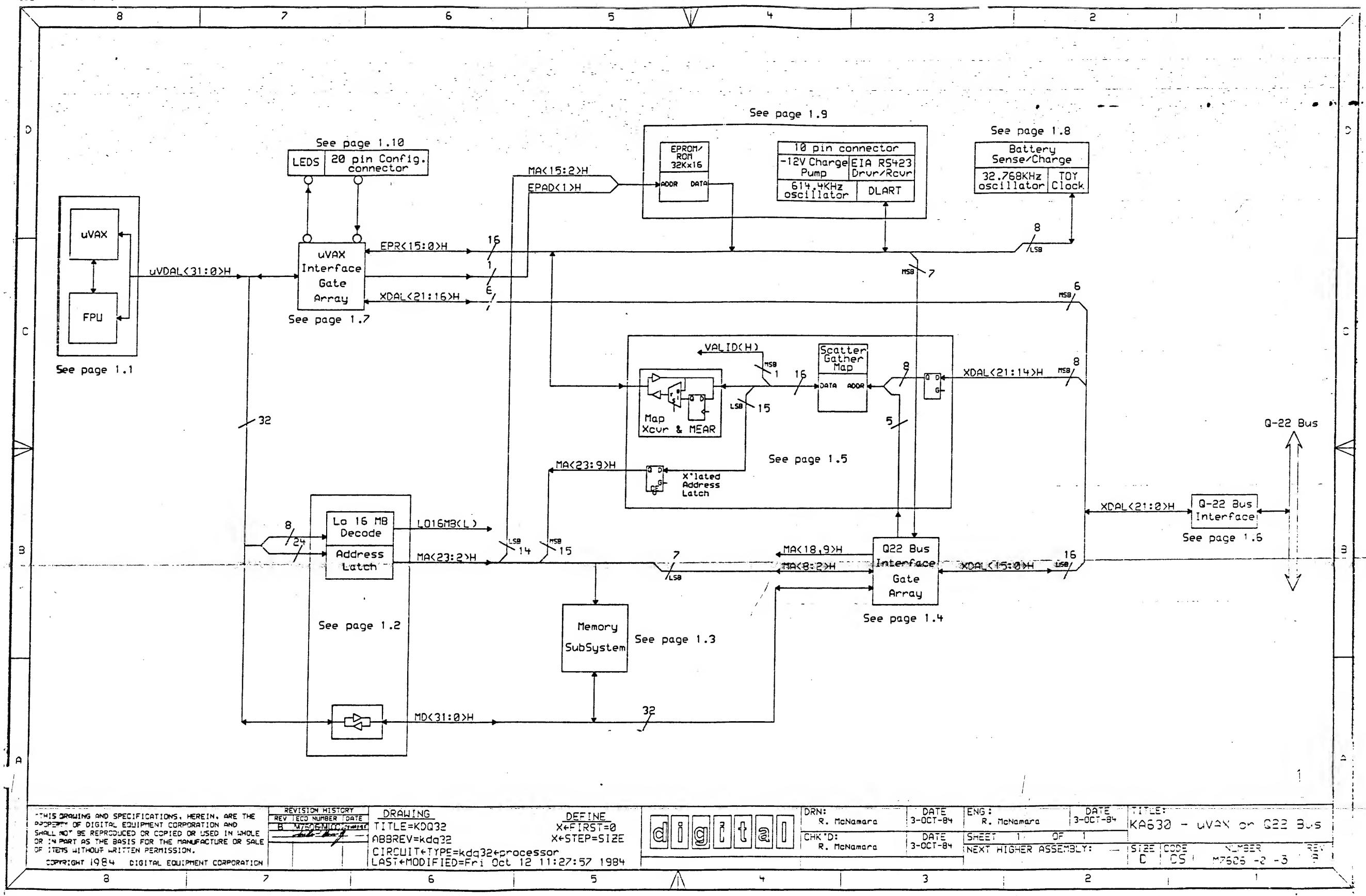
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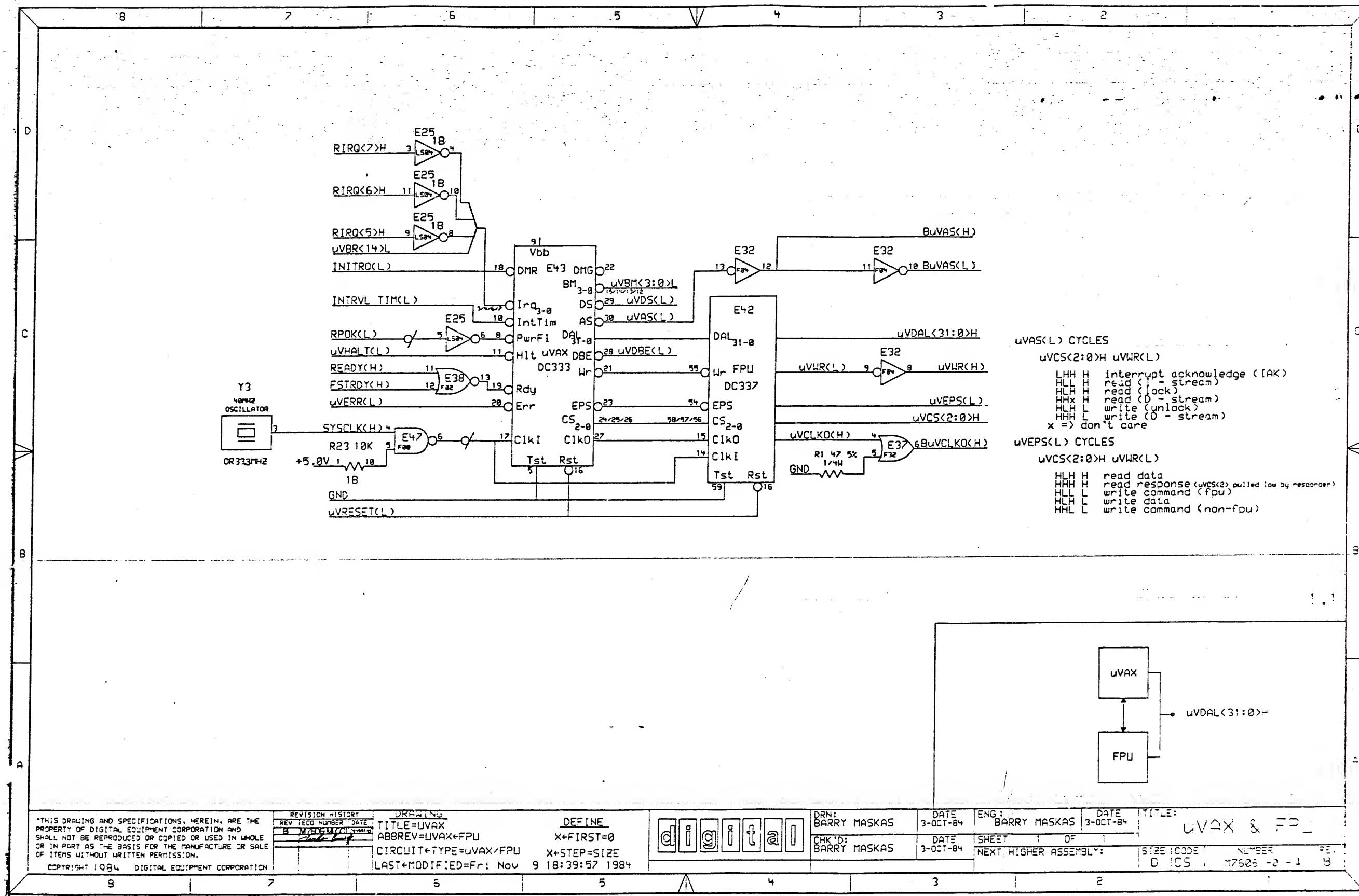
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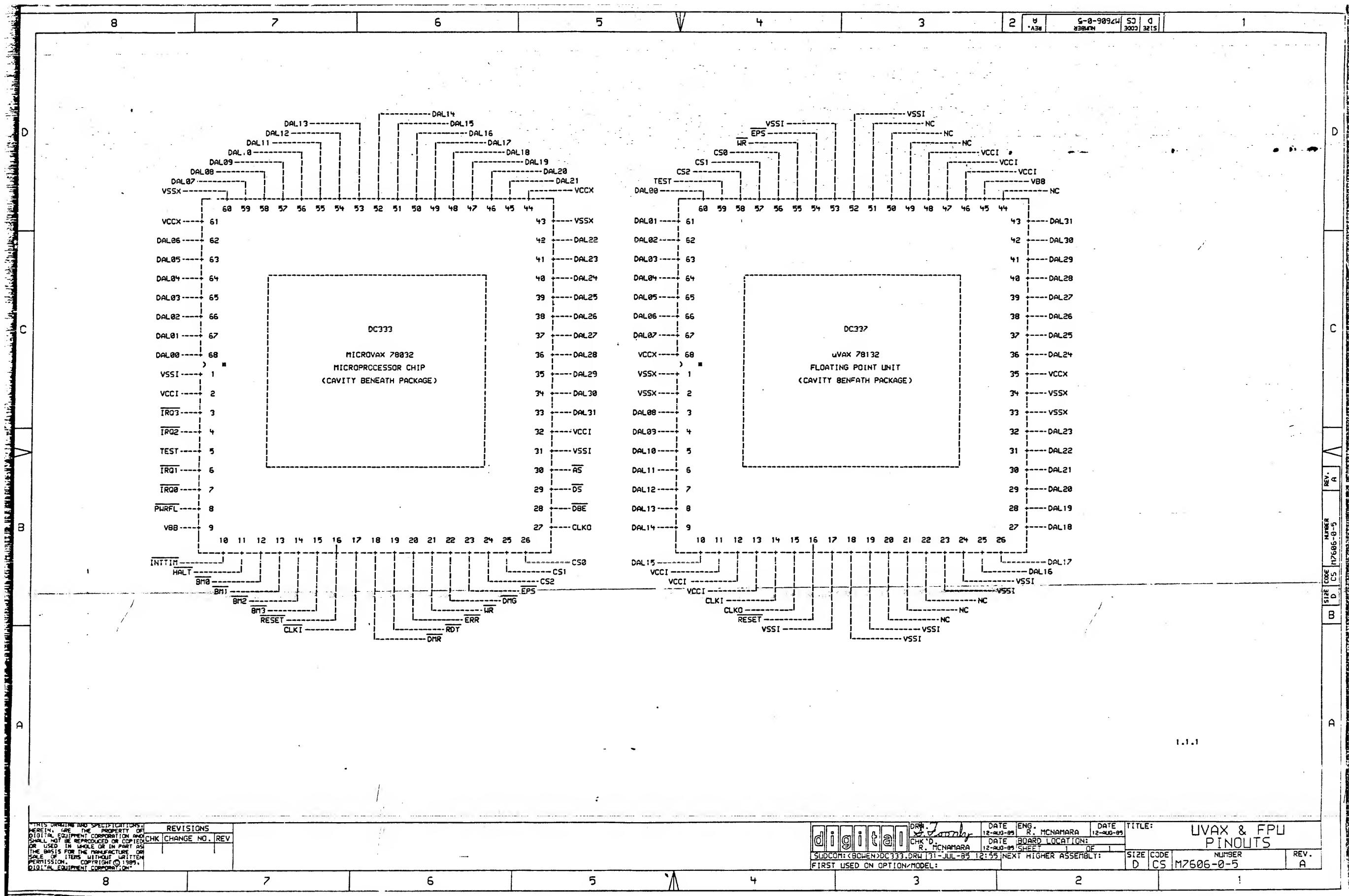
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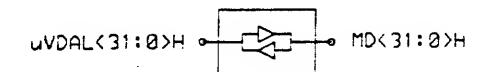
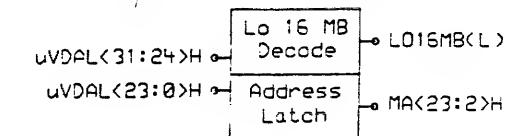
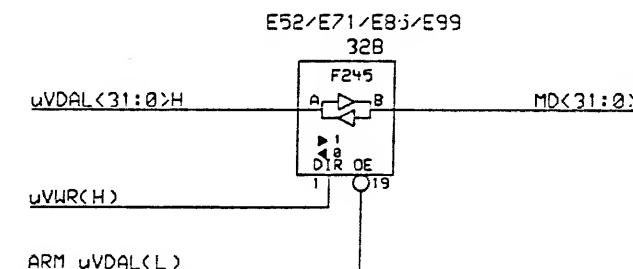
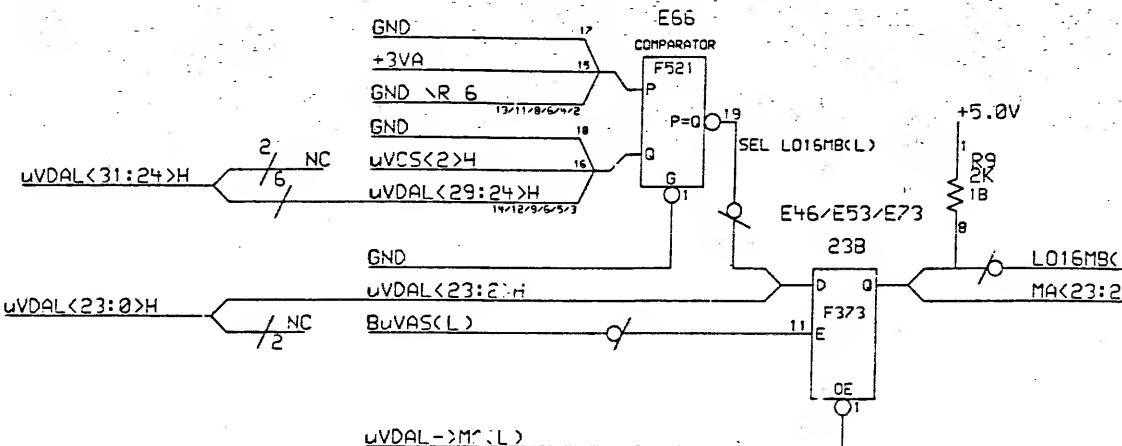
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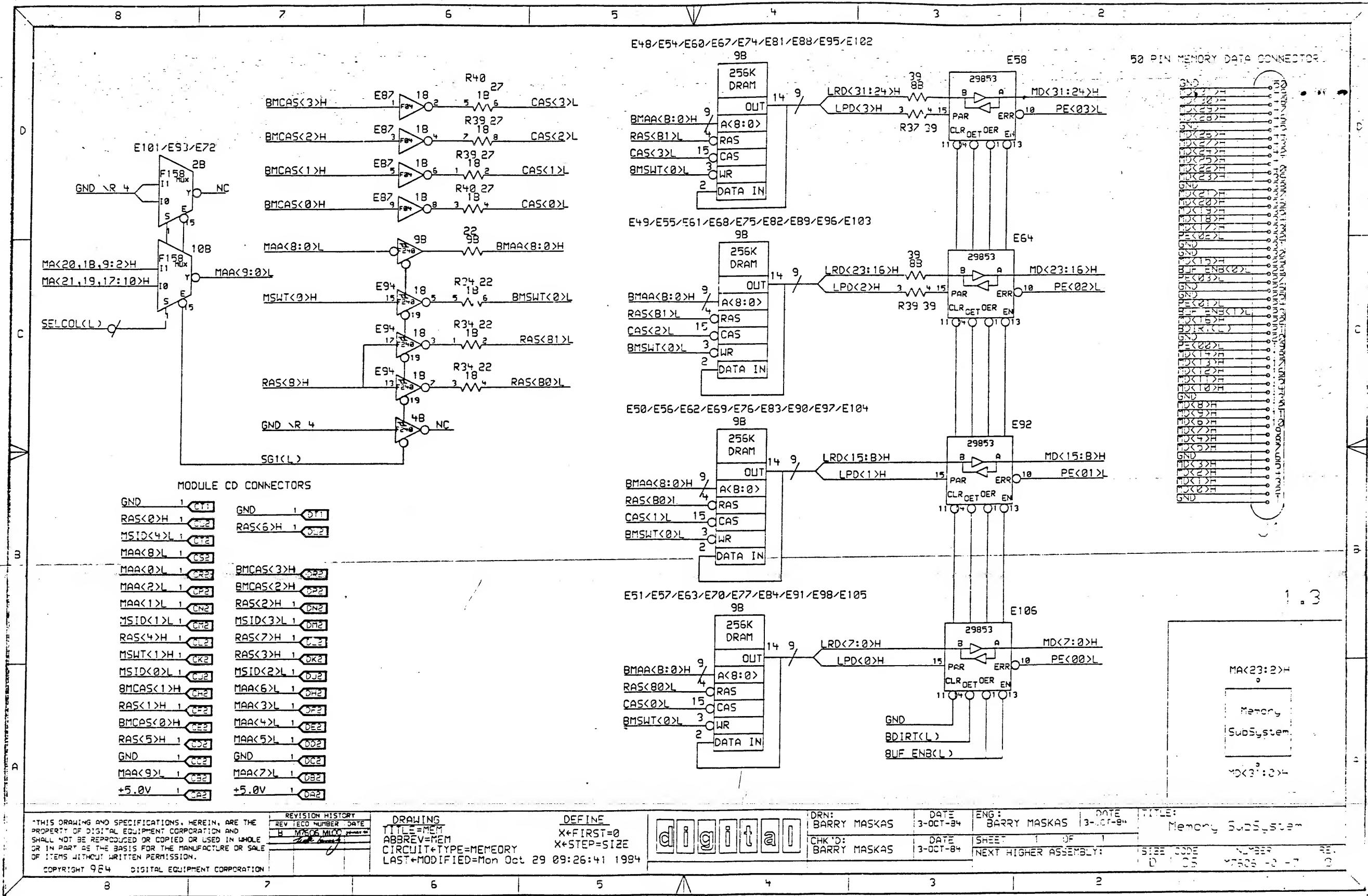


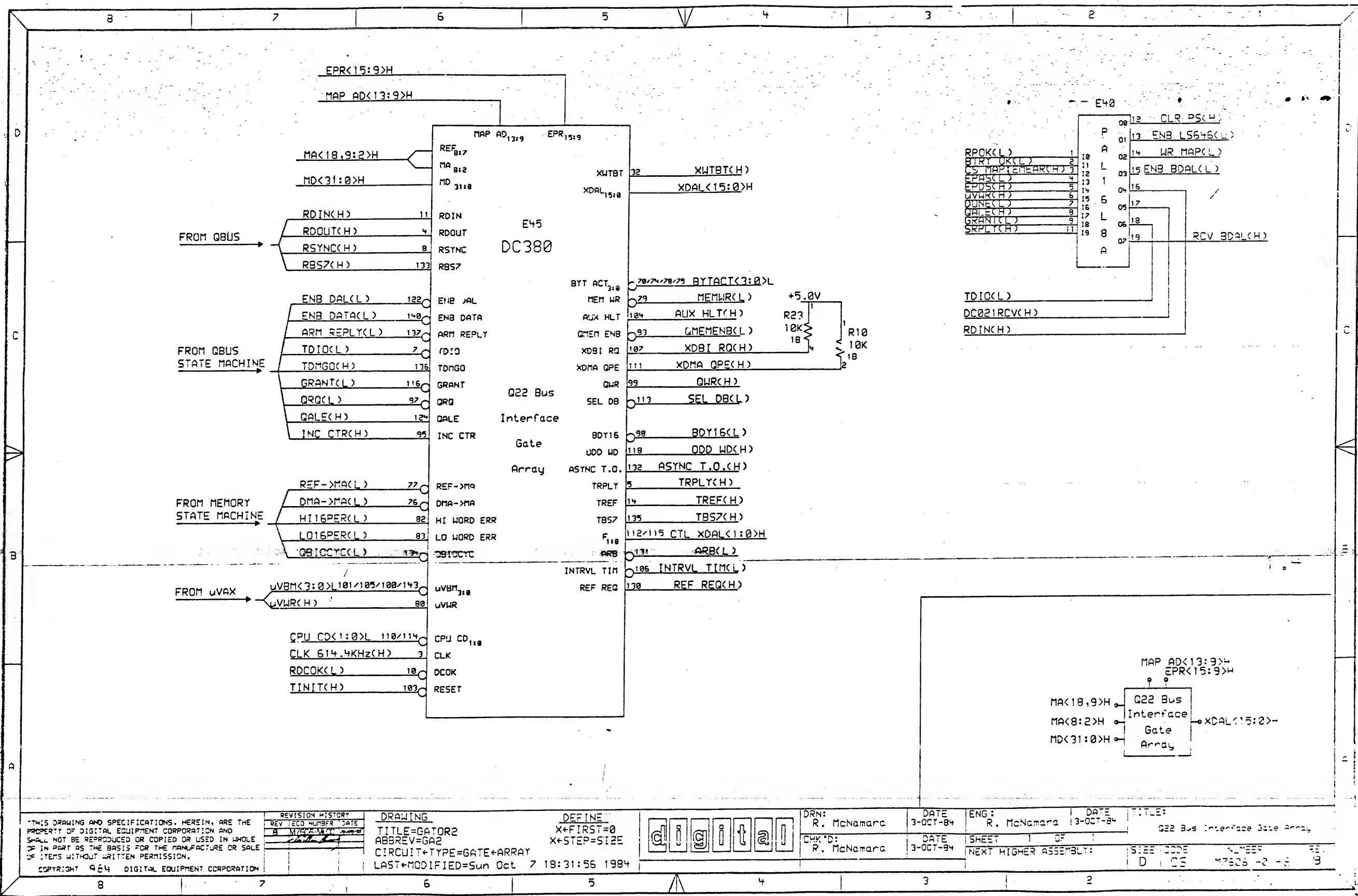












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REVISION HISTORY
REV ECO NUMBER DATE
9 MAC/AMC 1984

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LAST MODIFIED=Sun Oct 7 18:31:56 1984

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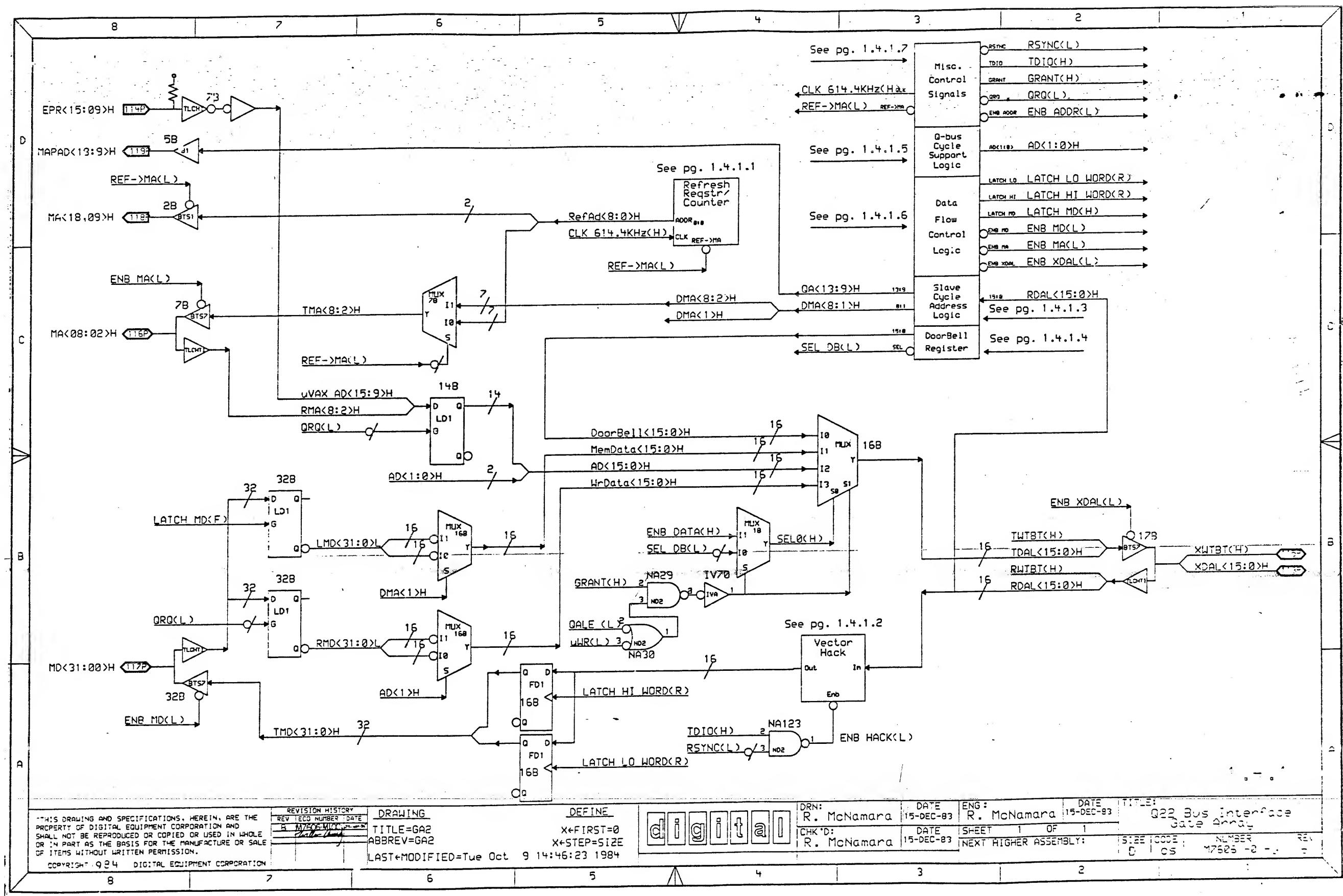
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CHK'D: R. McNamara

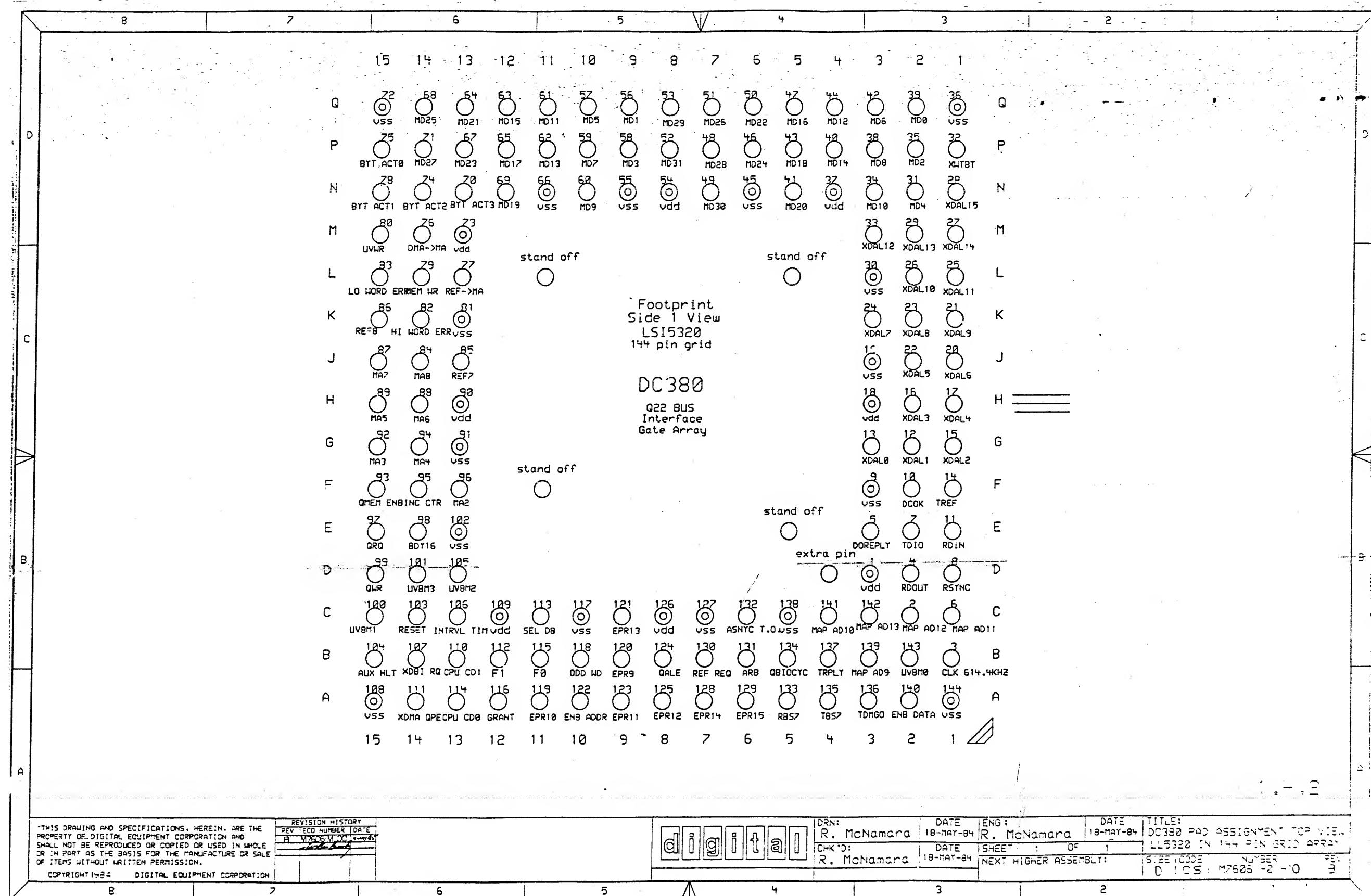
DATE: 3-OCT-84
DATE: 3-OCT-84

ENG: R. McNamara
SHEET 1 OF 1

DATE: 3-OCT-84
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SIZE CODE NUMBER REV
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d i g i t a

DRN:
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CHK'D:
P. M

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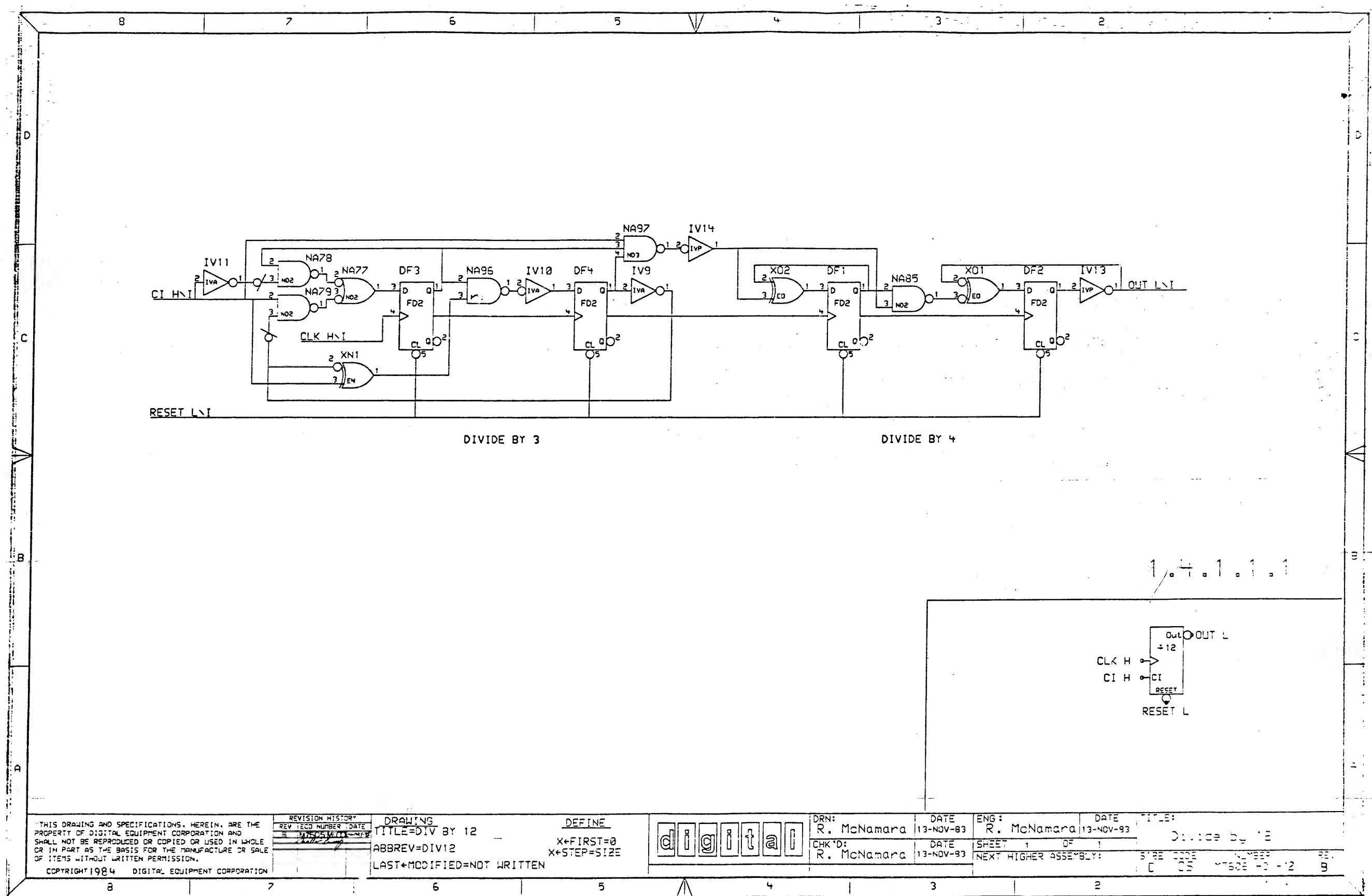
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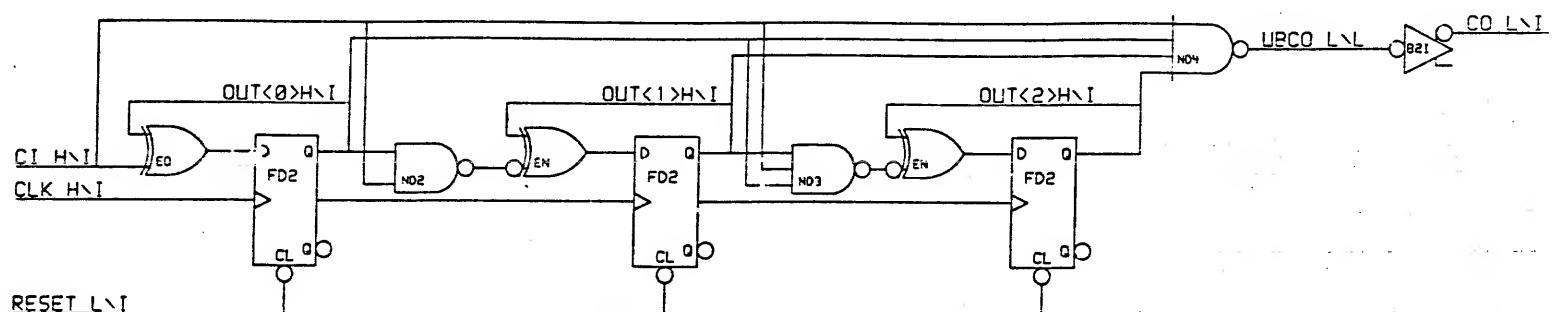
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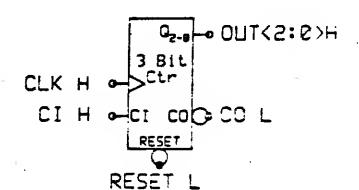
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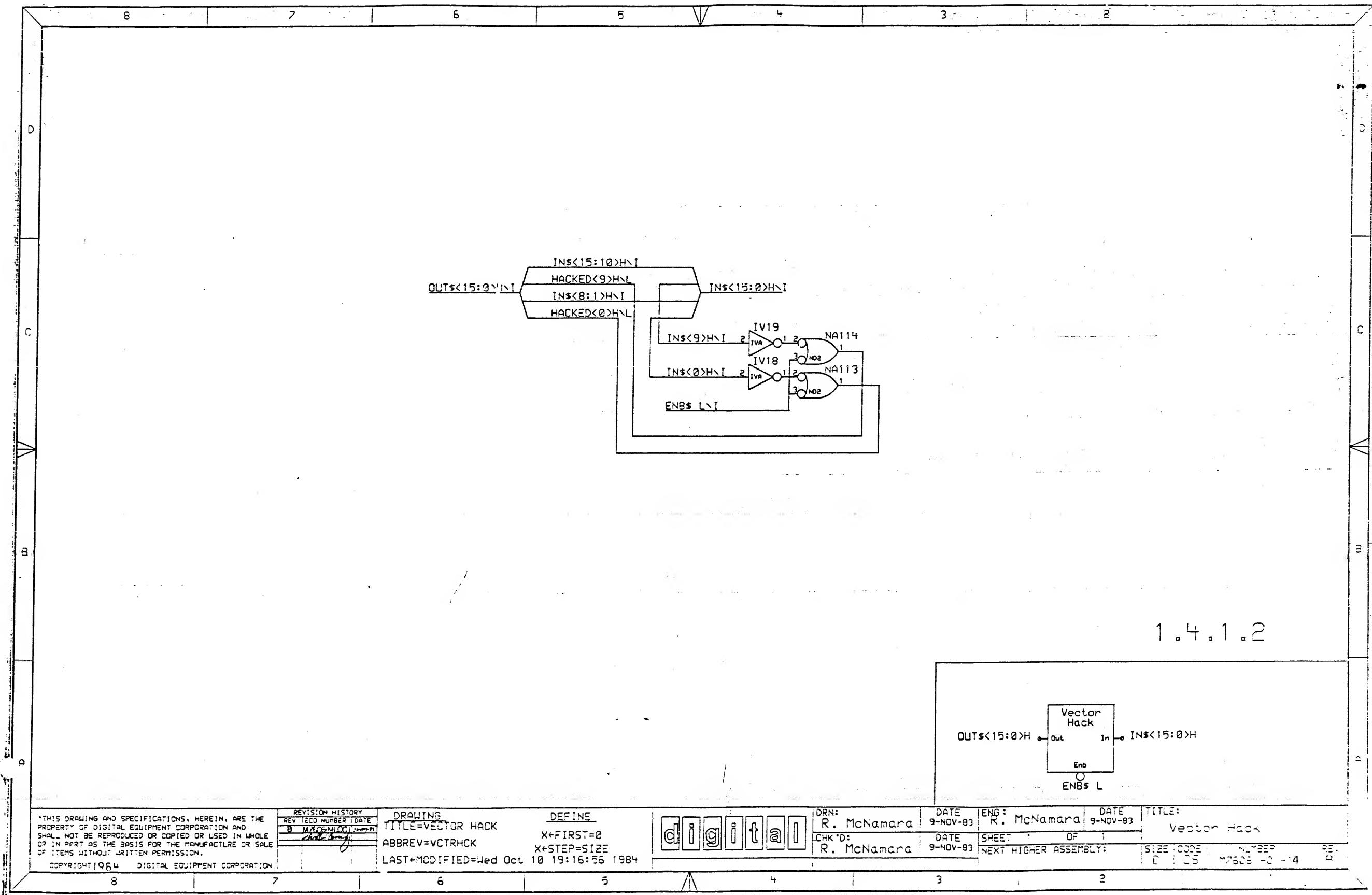


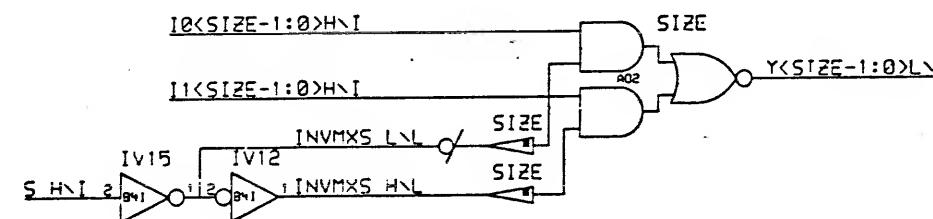


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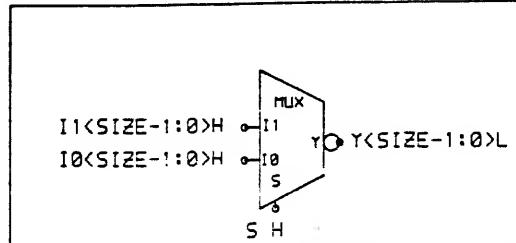


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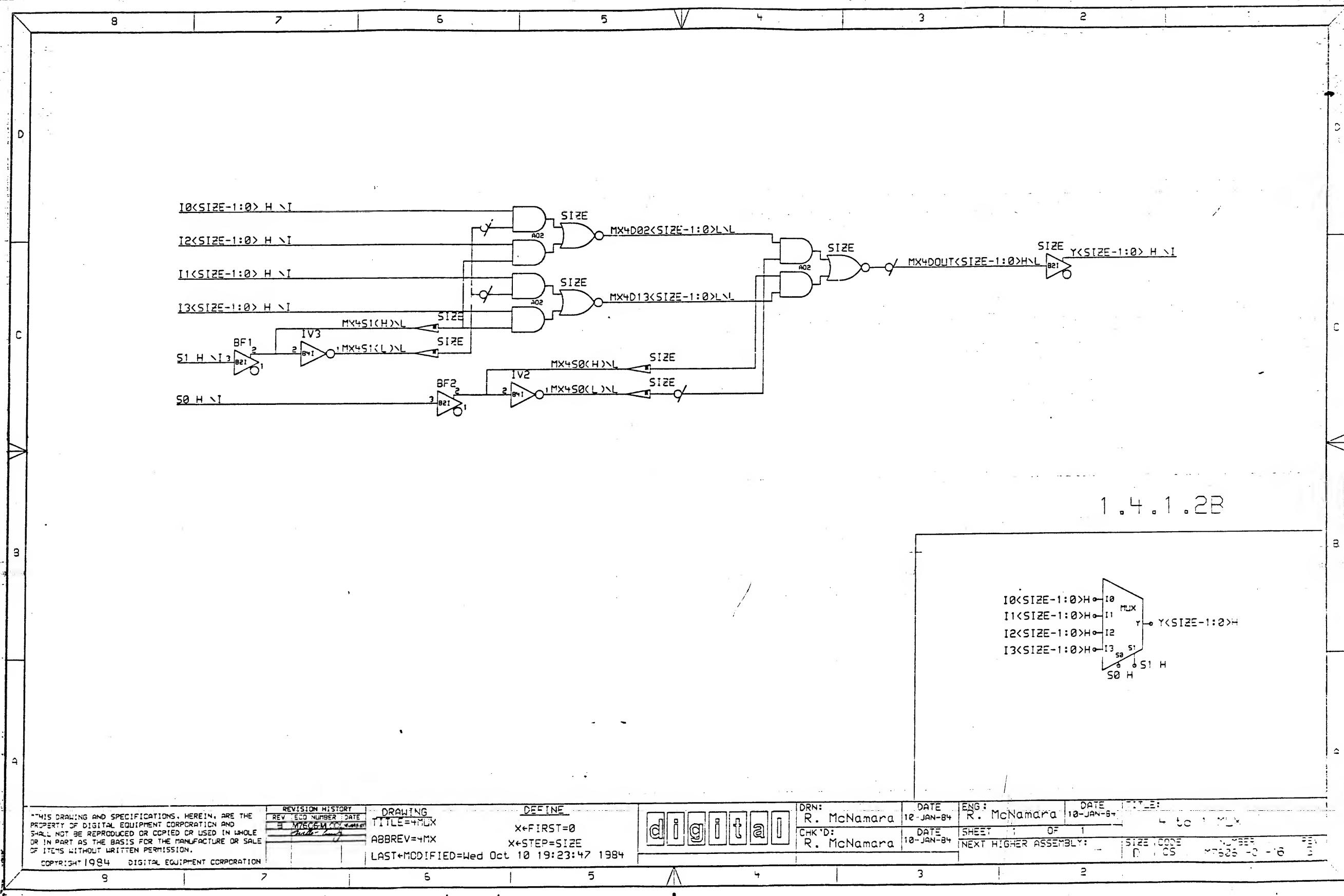


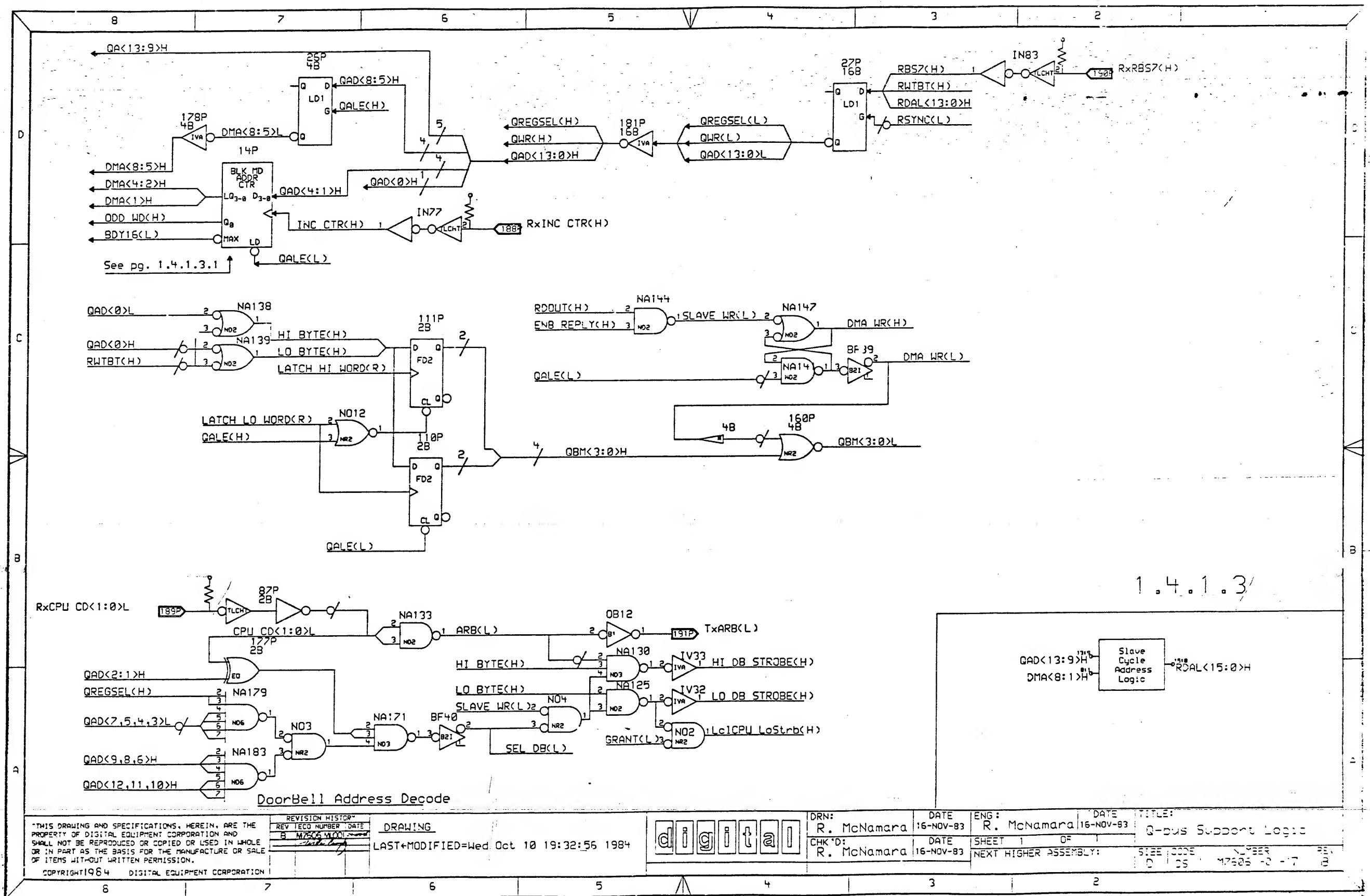


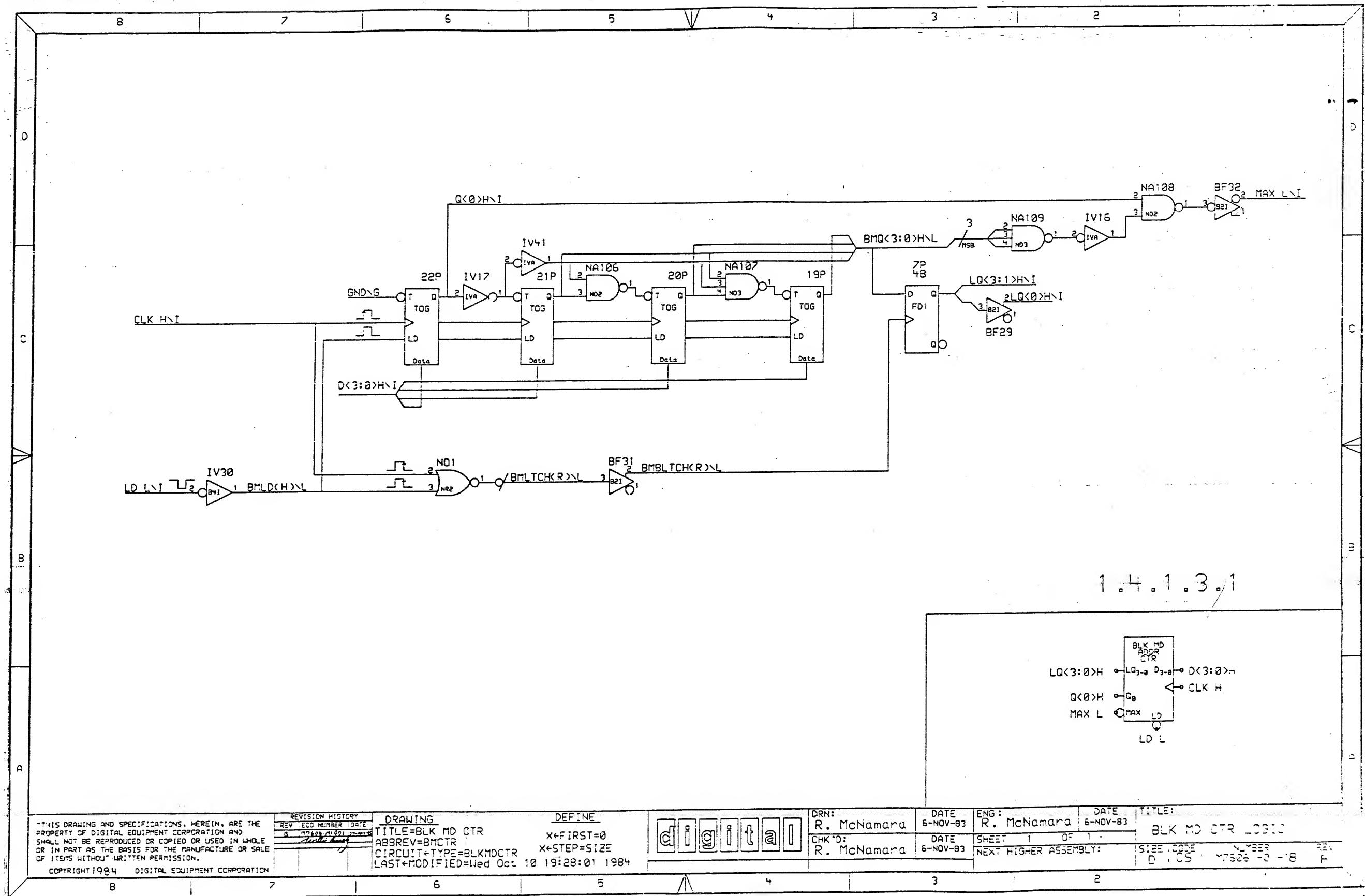
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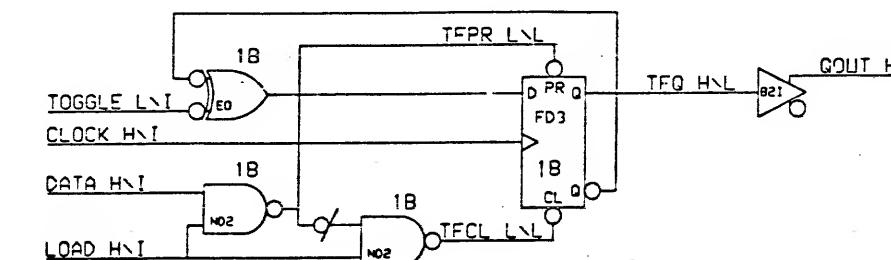


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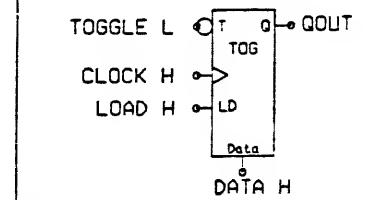




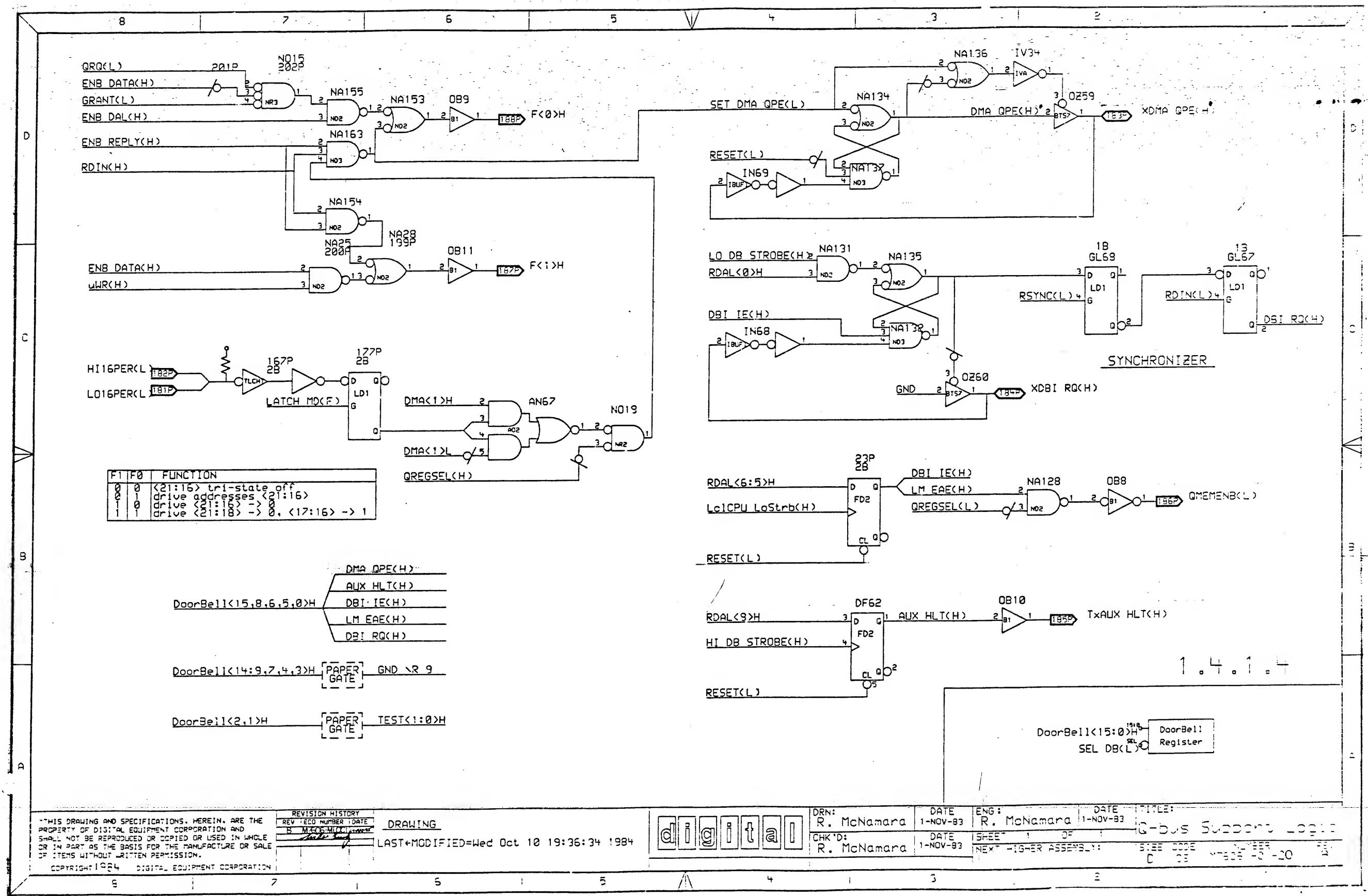


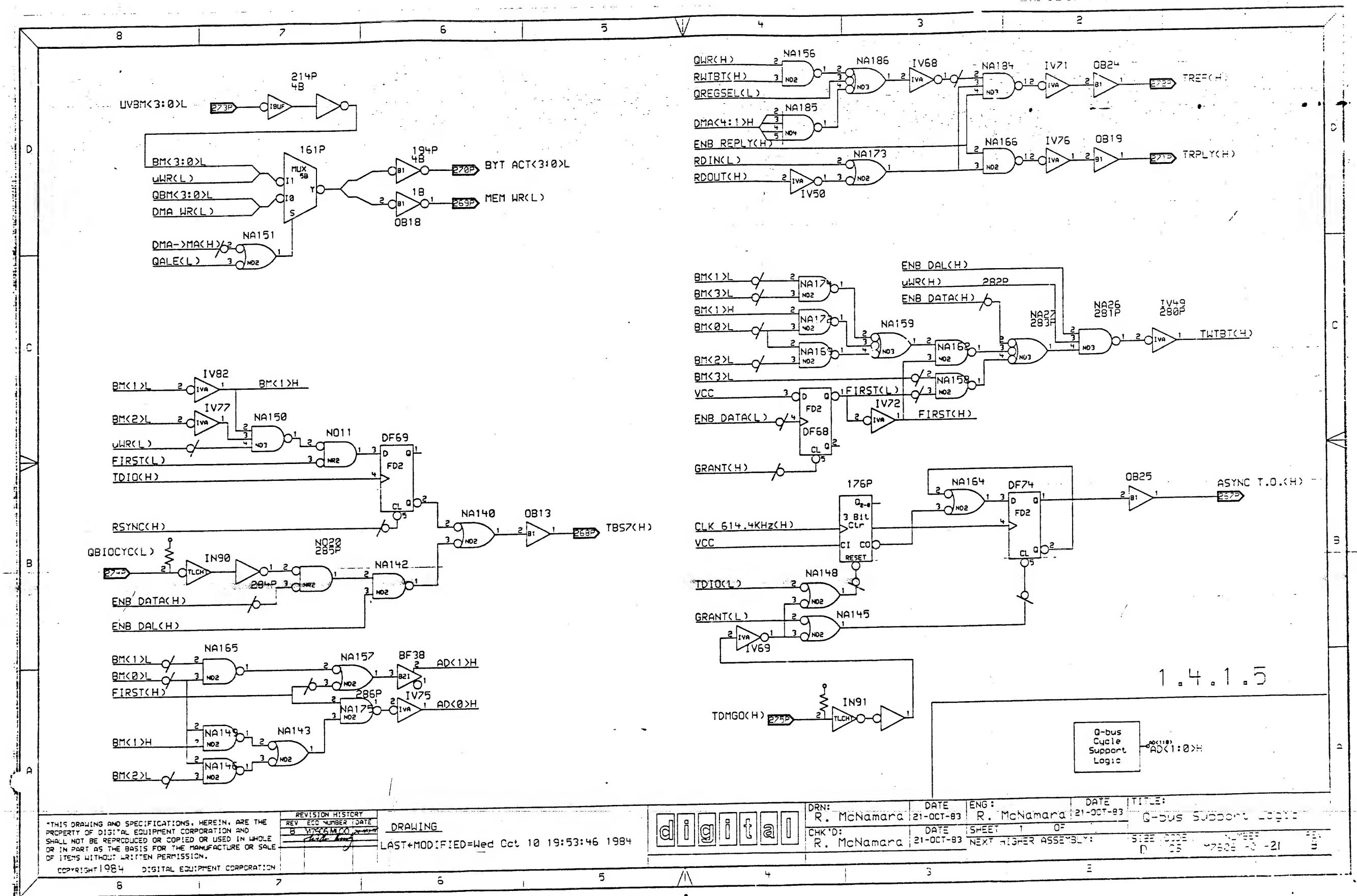


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REVISION HISTORY			DEFINITION	DRN:	DATE	ENG:	DATE	TITLE:
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				R. McNamara	16-NOV-83			NEXT HIGHER ASSEMBLY:
ABBREV=TOG			LAST+MODIFIED=Wed Oct 10 19:57:28 1984					STEE CODE
Copyright 1984 DIGITAL EQUIPMENT CORPORATION								17825-01-01





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REV ECO NUMBER DATE

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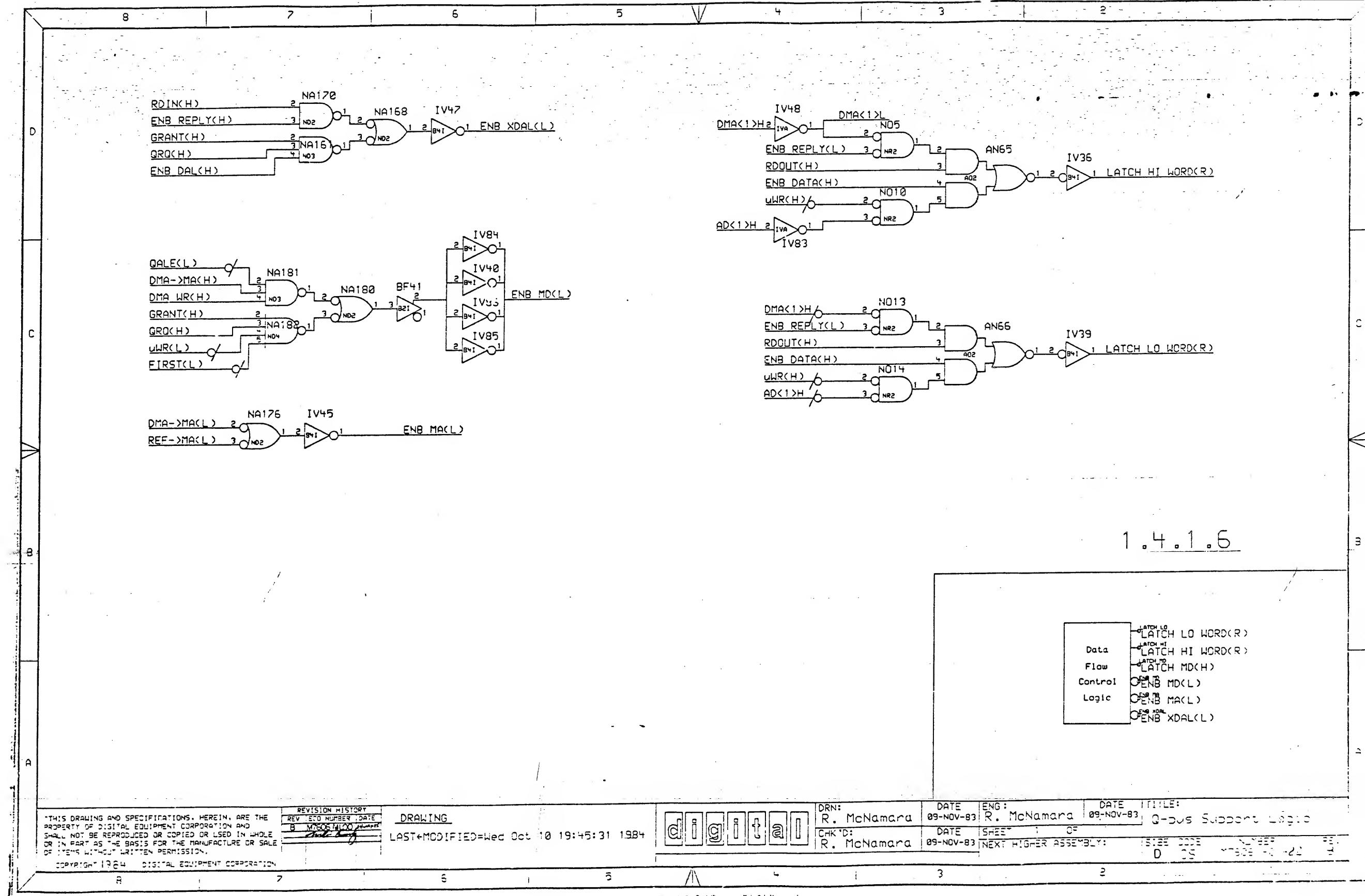
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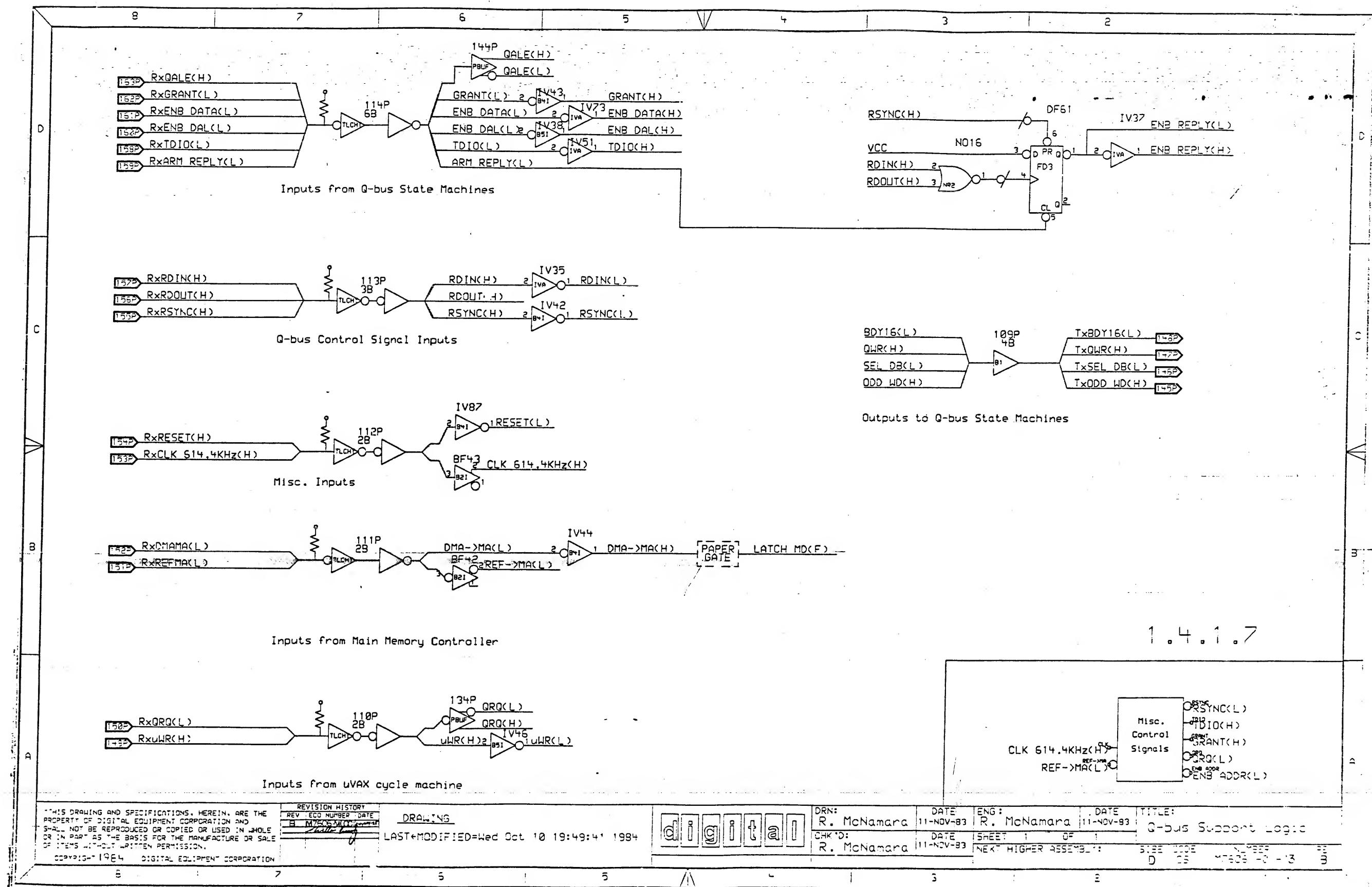
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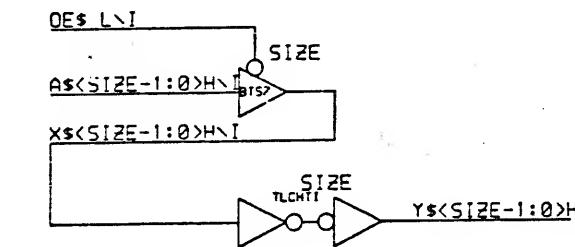
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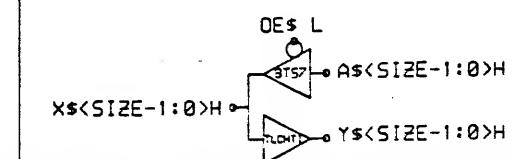
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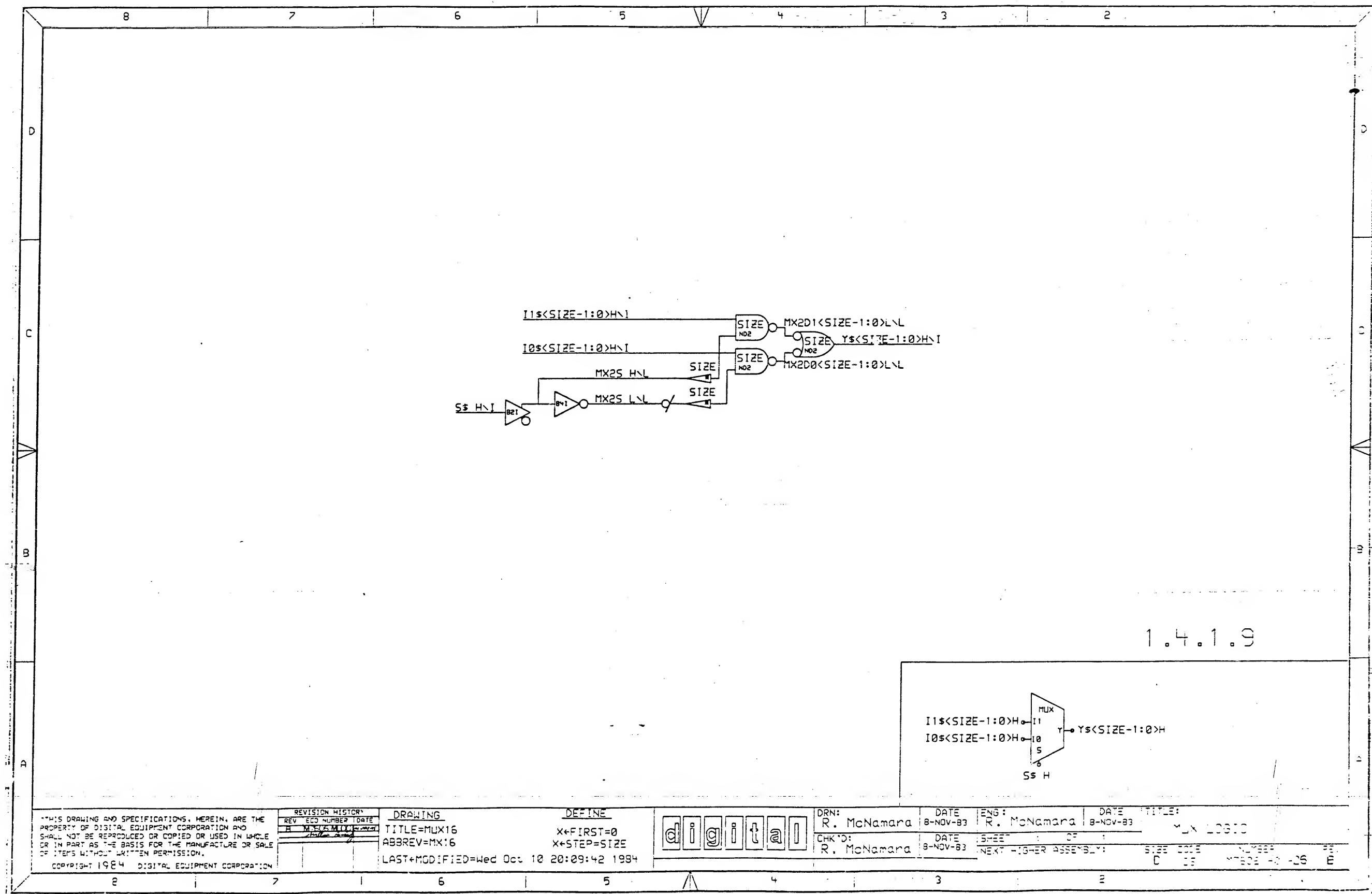
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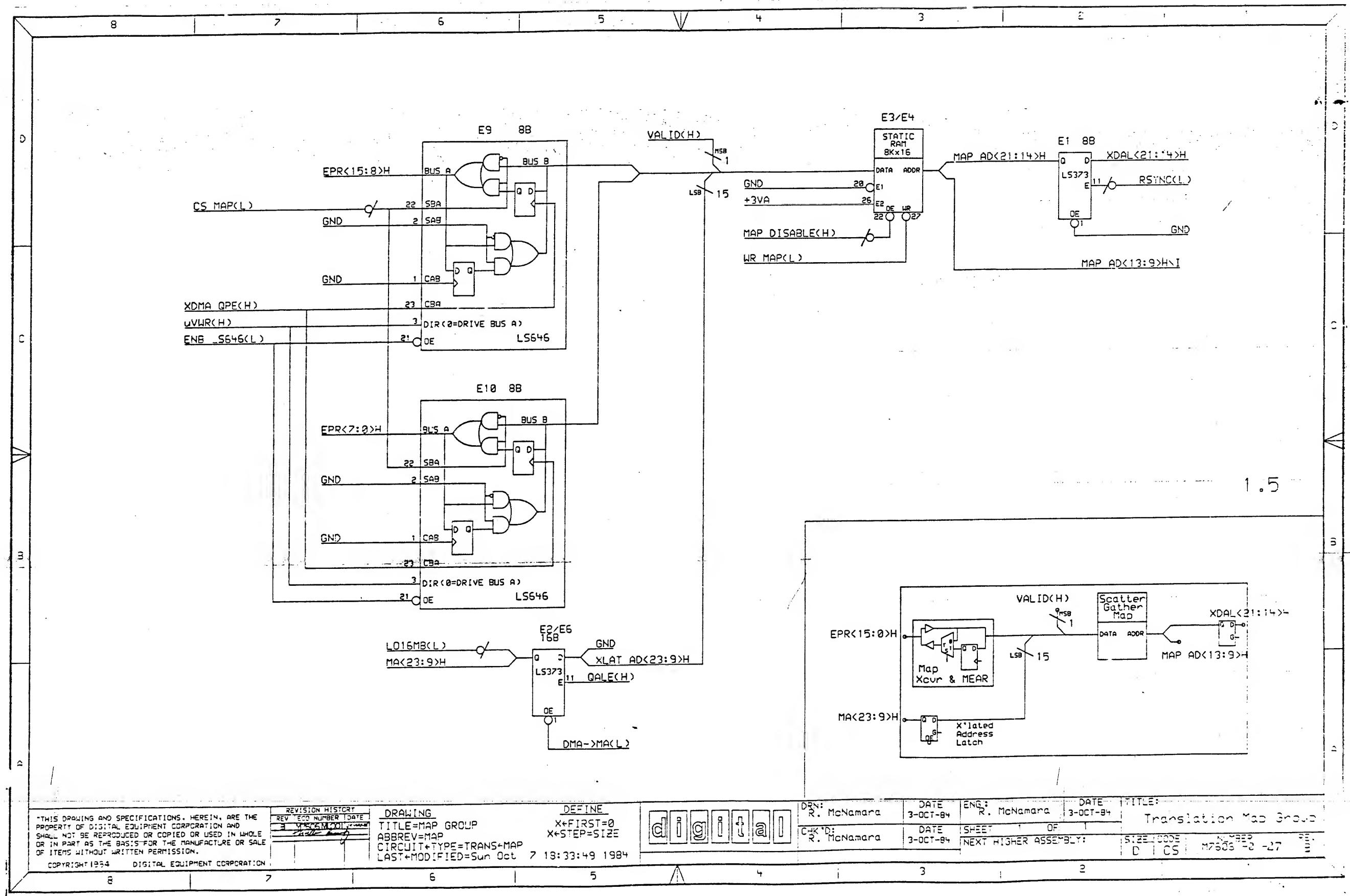
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		B 10000000000000000000000000000000	ABBREV=PBUF	X<STEP=SIZE	CHK'D:	DATE	ISHEET	OF	
			LAST<MODIFIED=Wed Oct 10 20:01:17 1984	R. McNamara	11-JAN-84	1	1		
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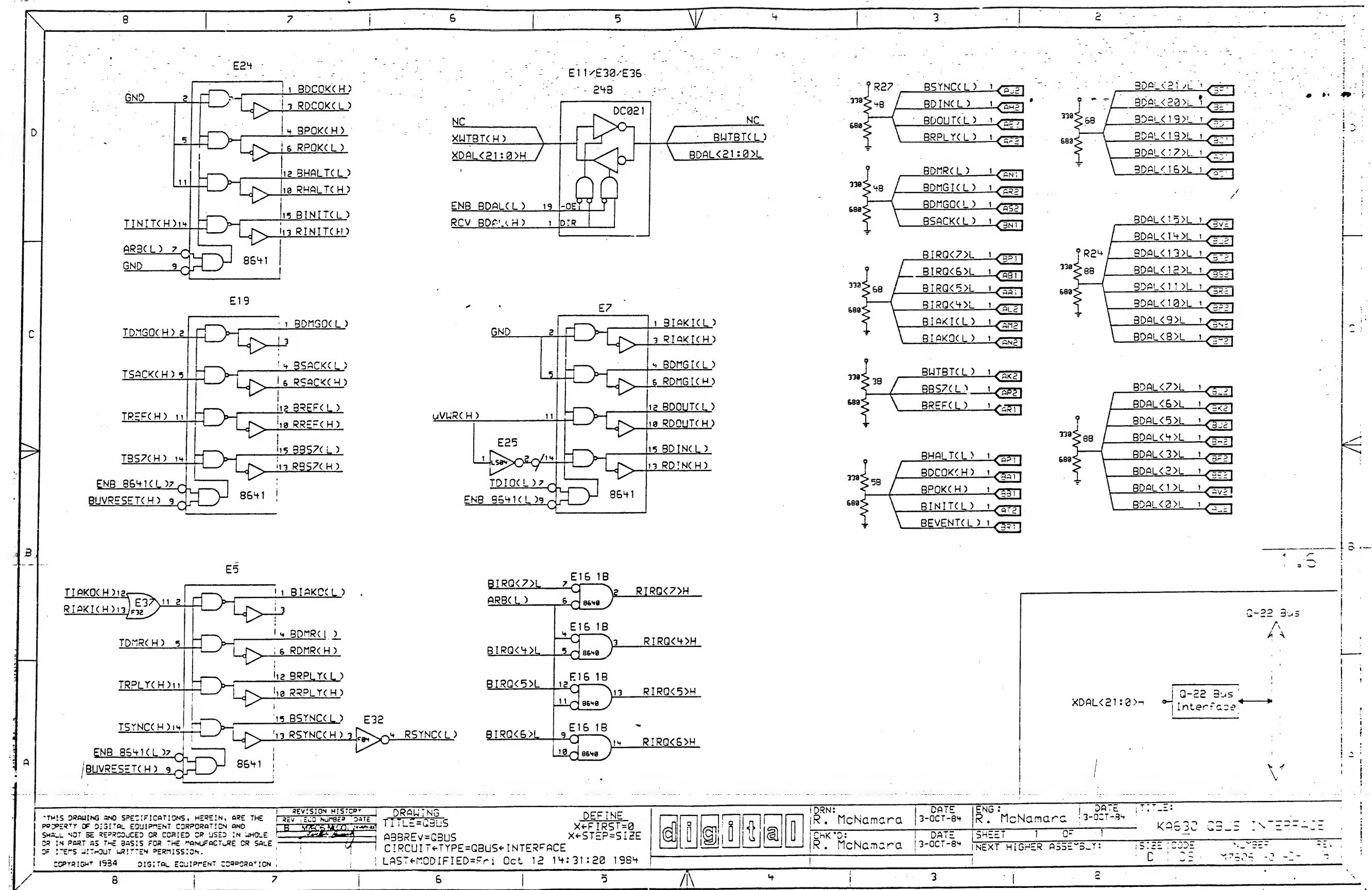


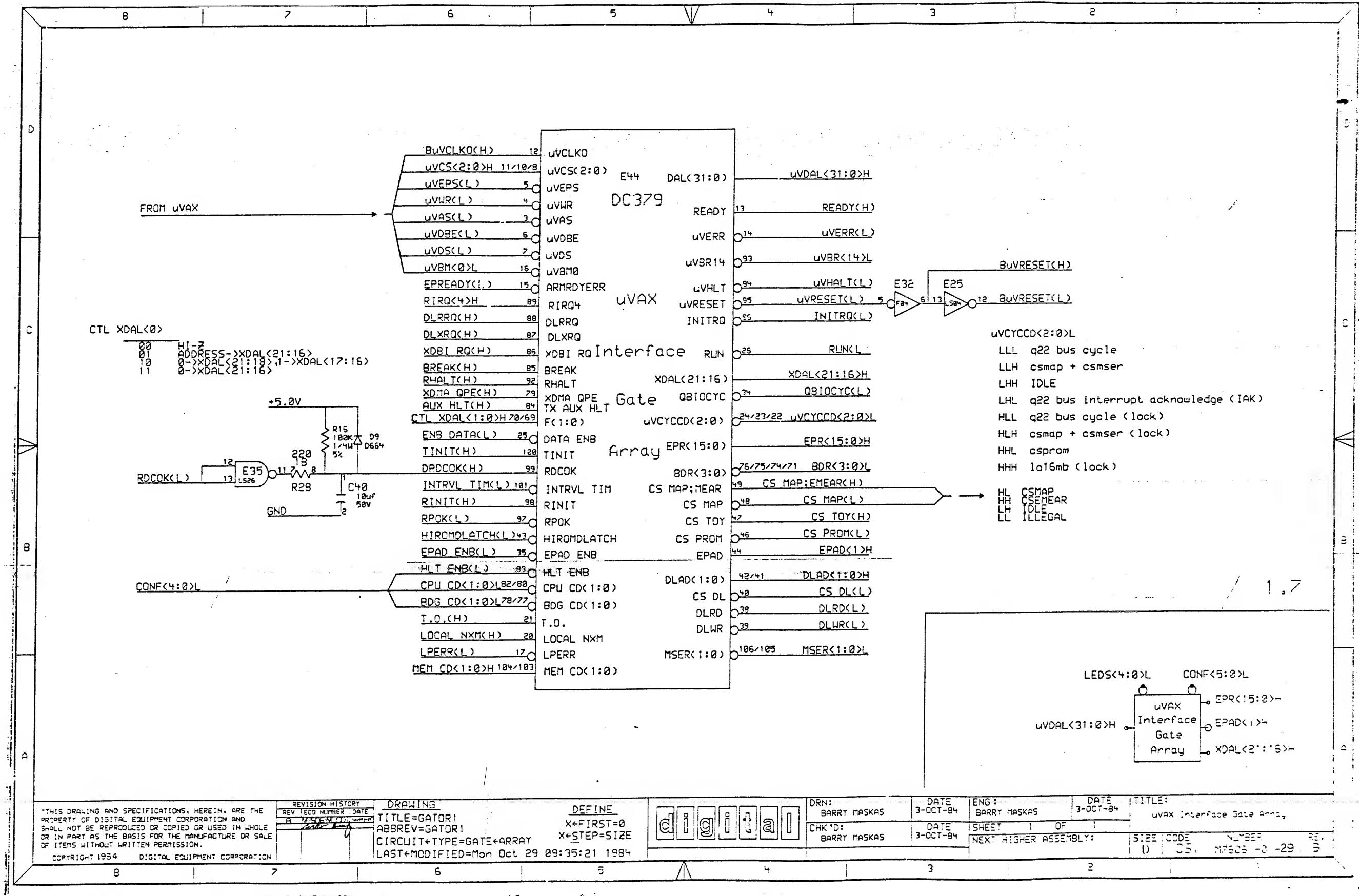
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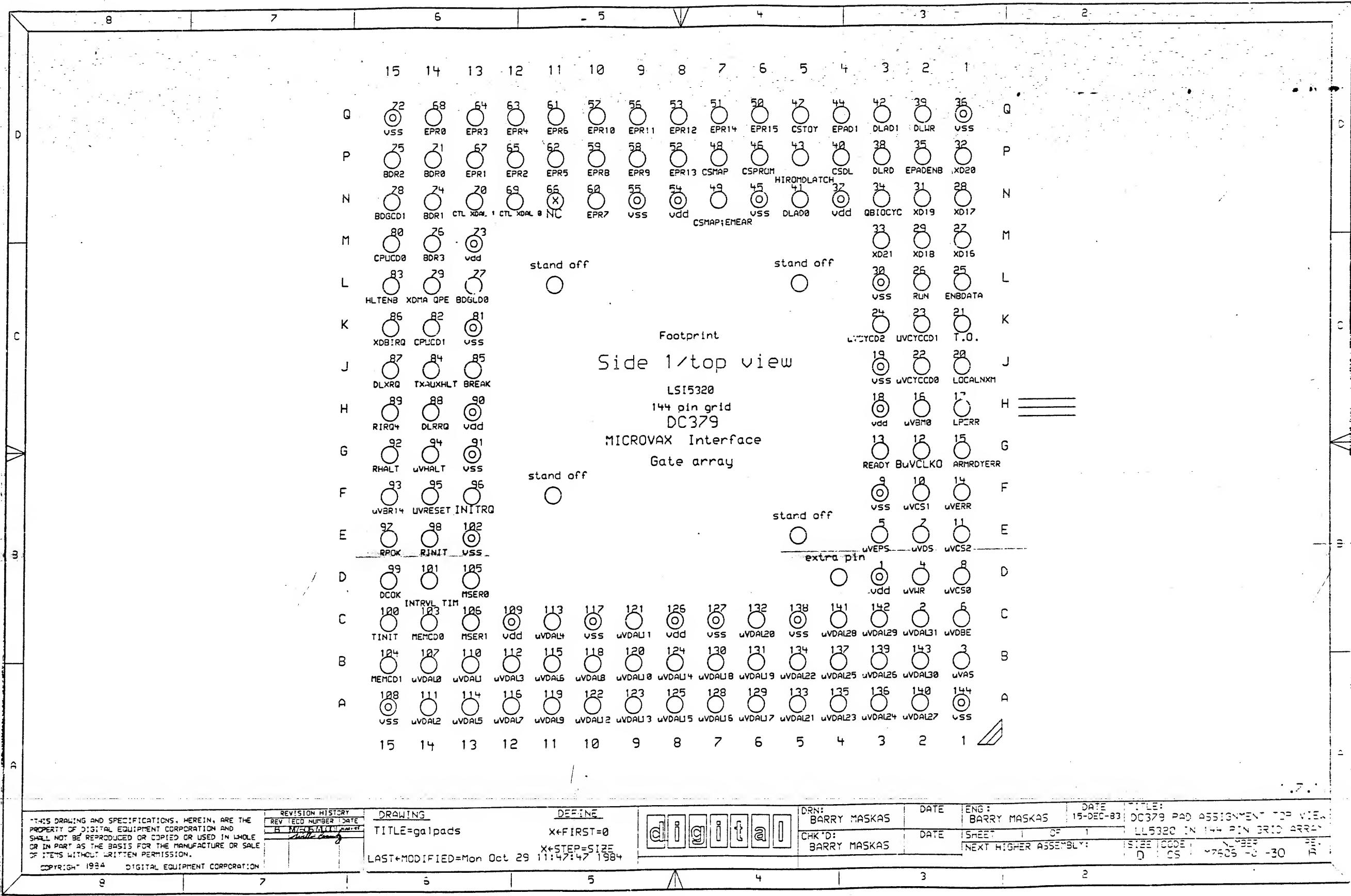


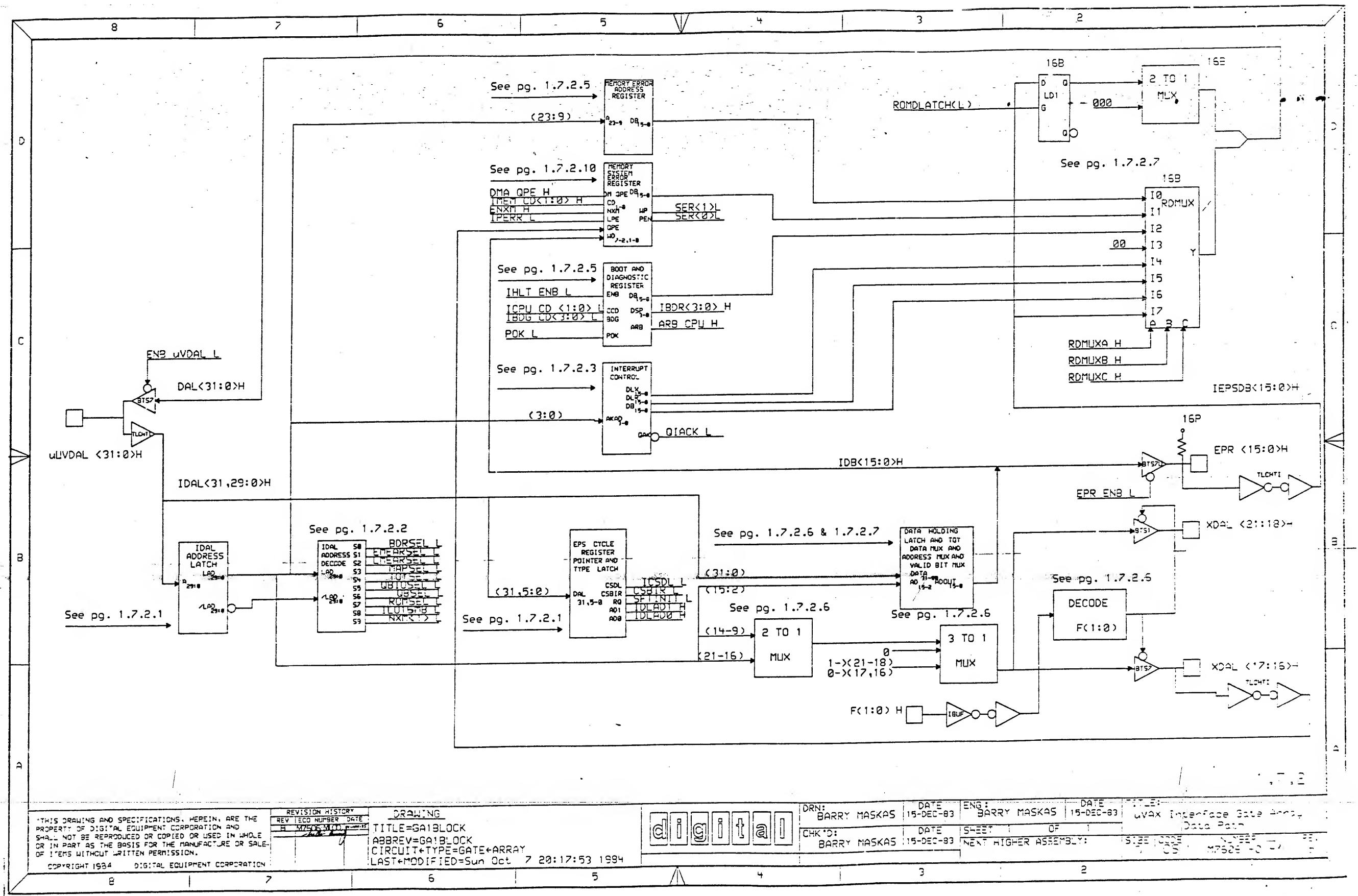


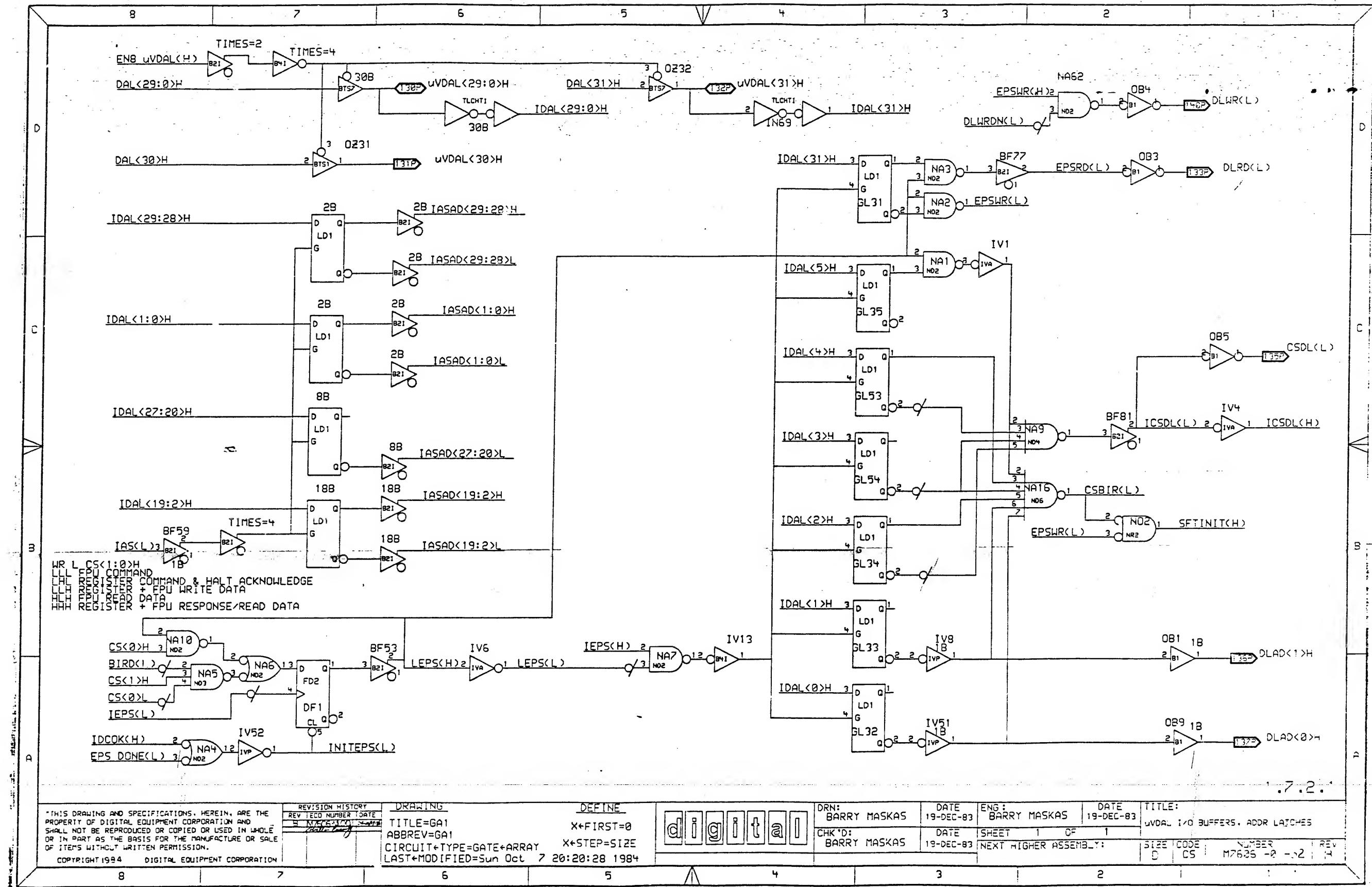


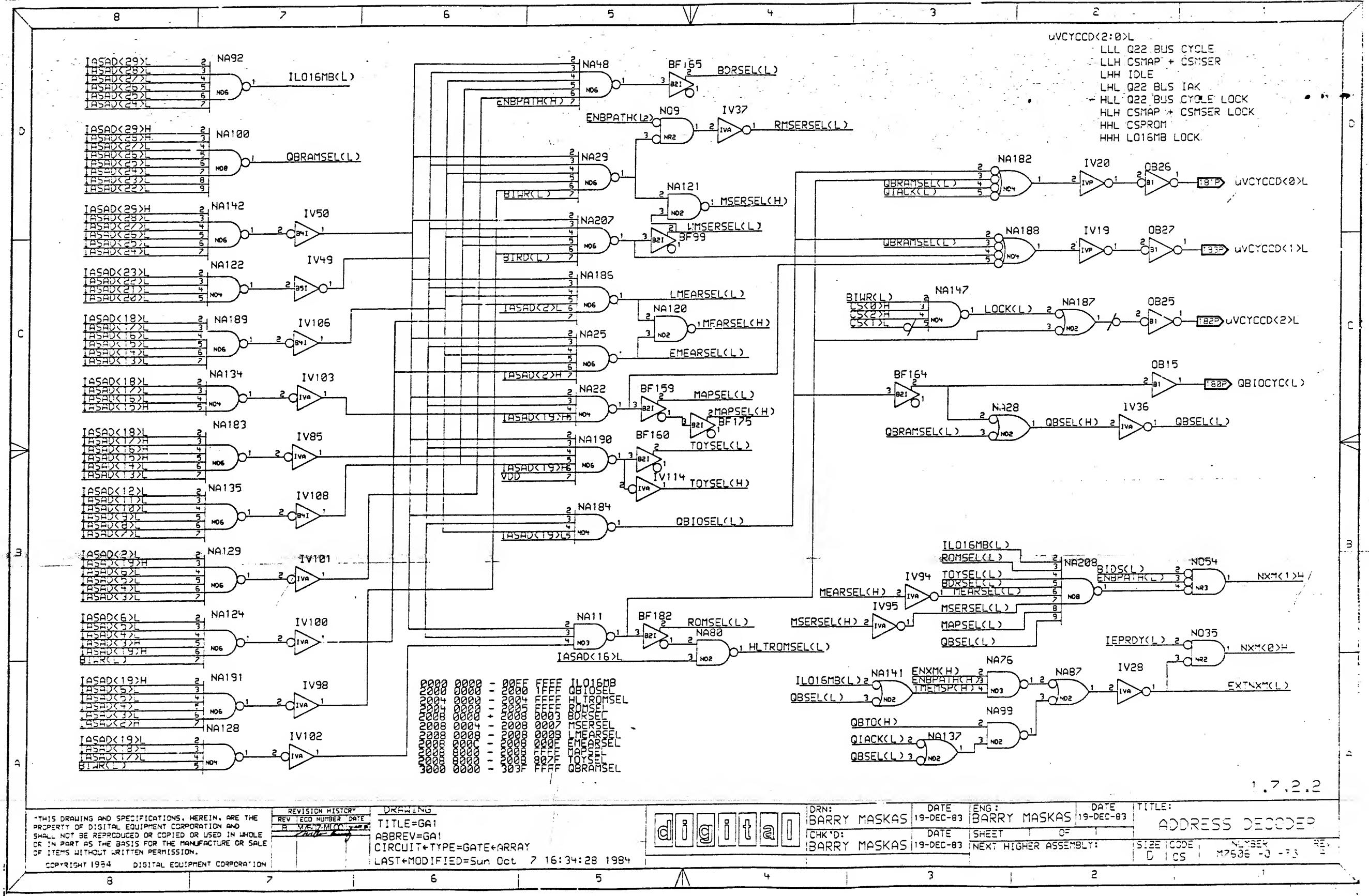


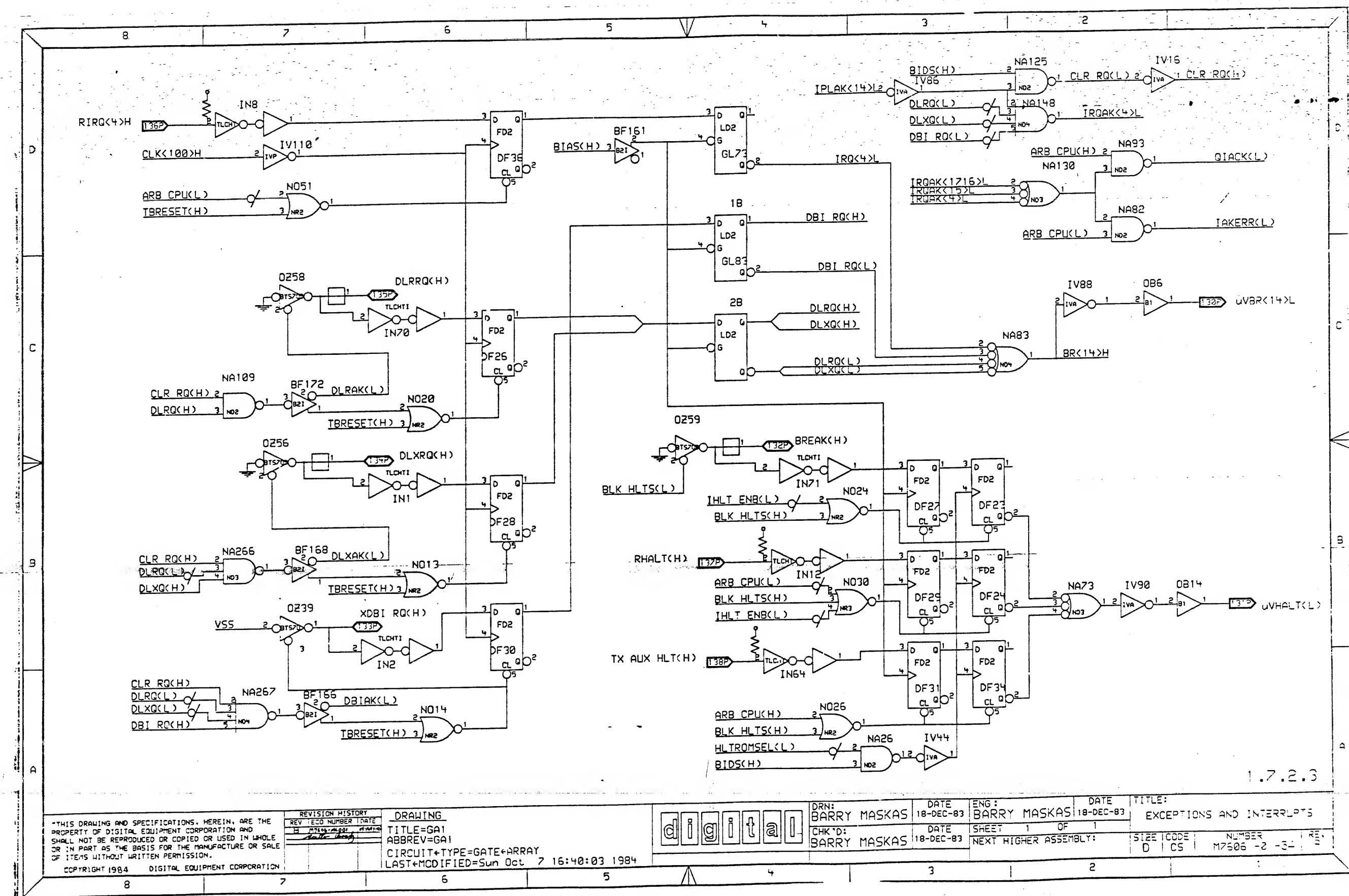






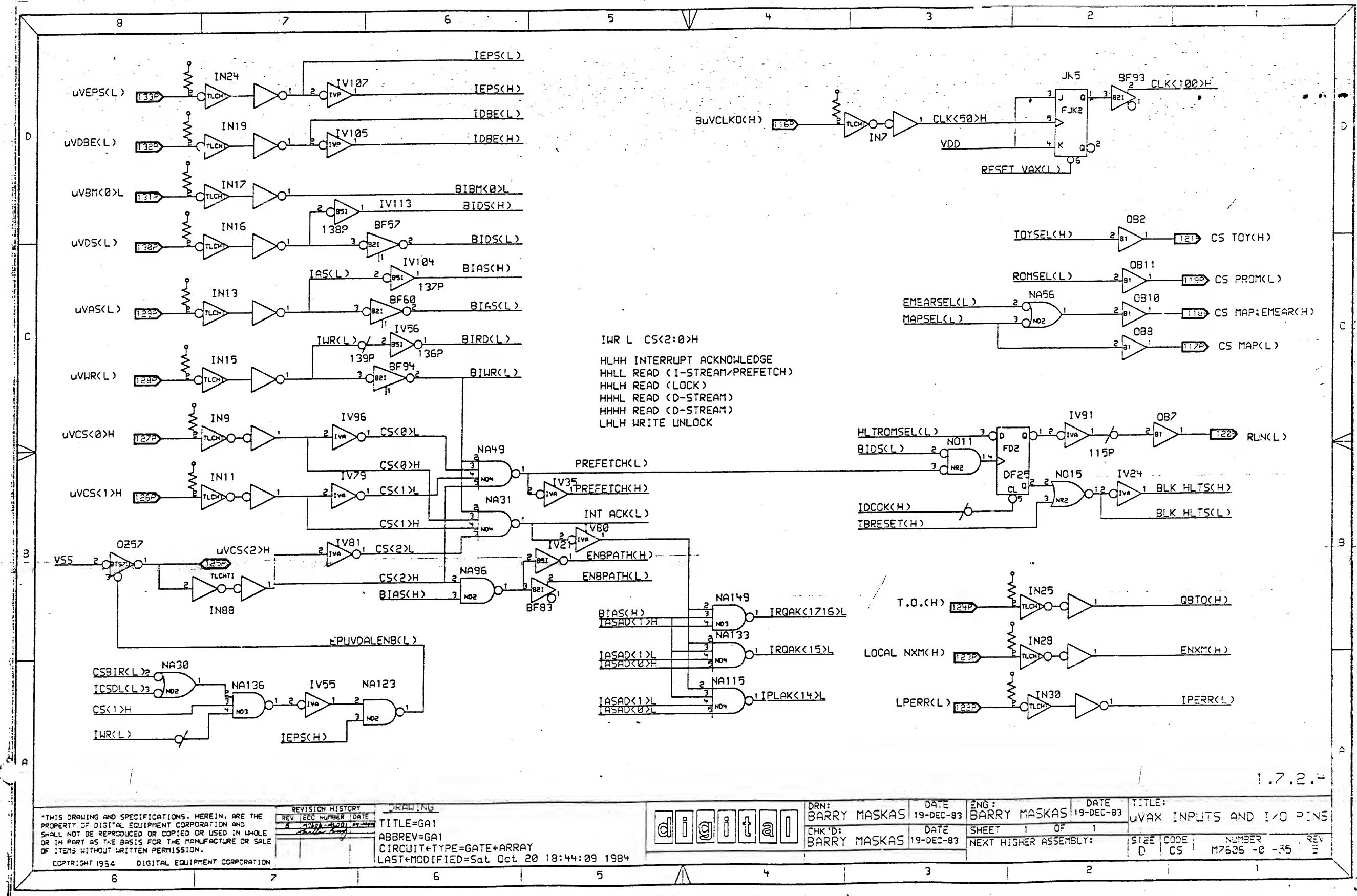


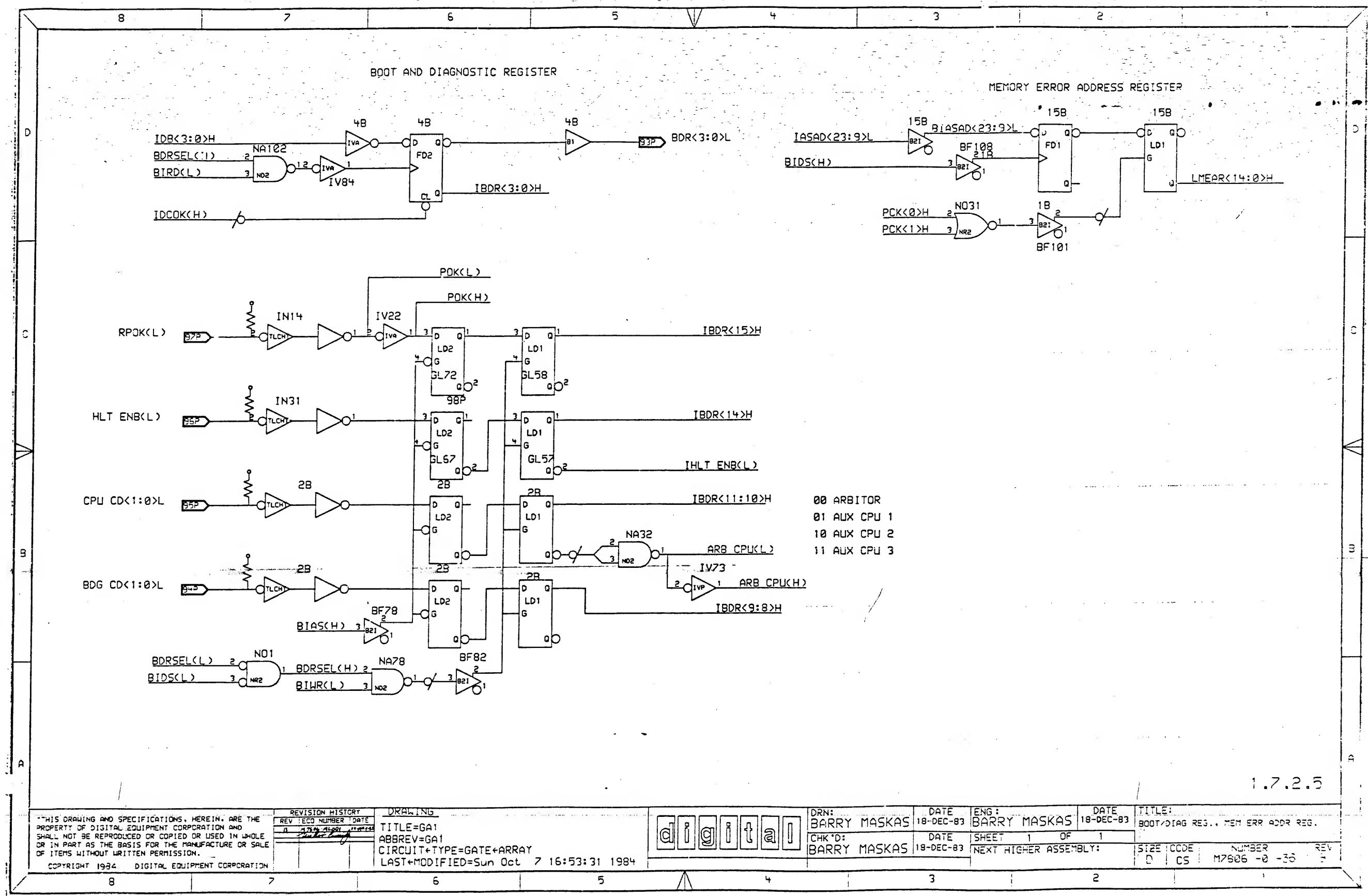


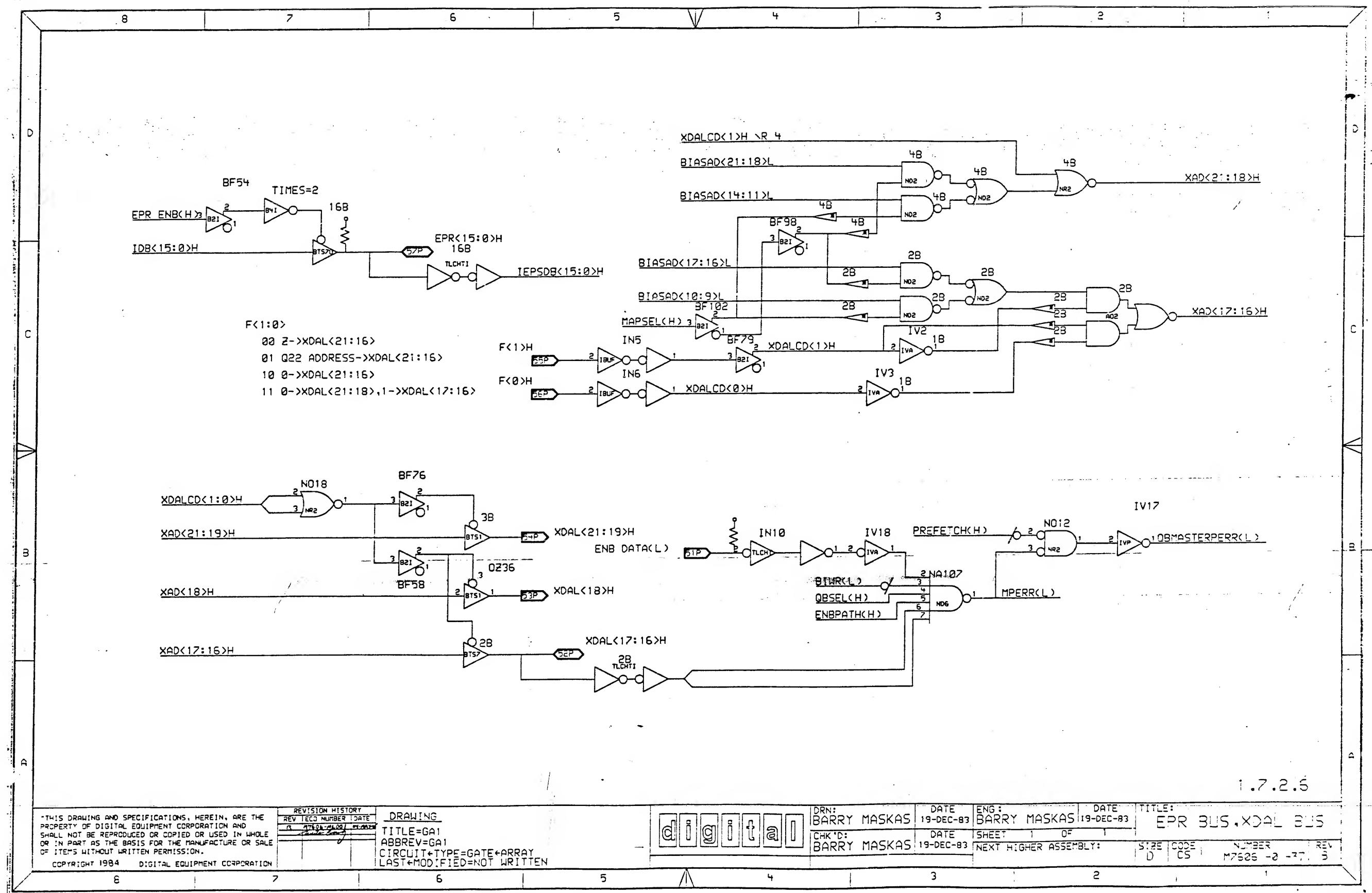


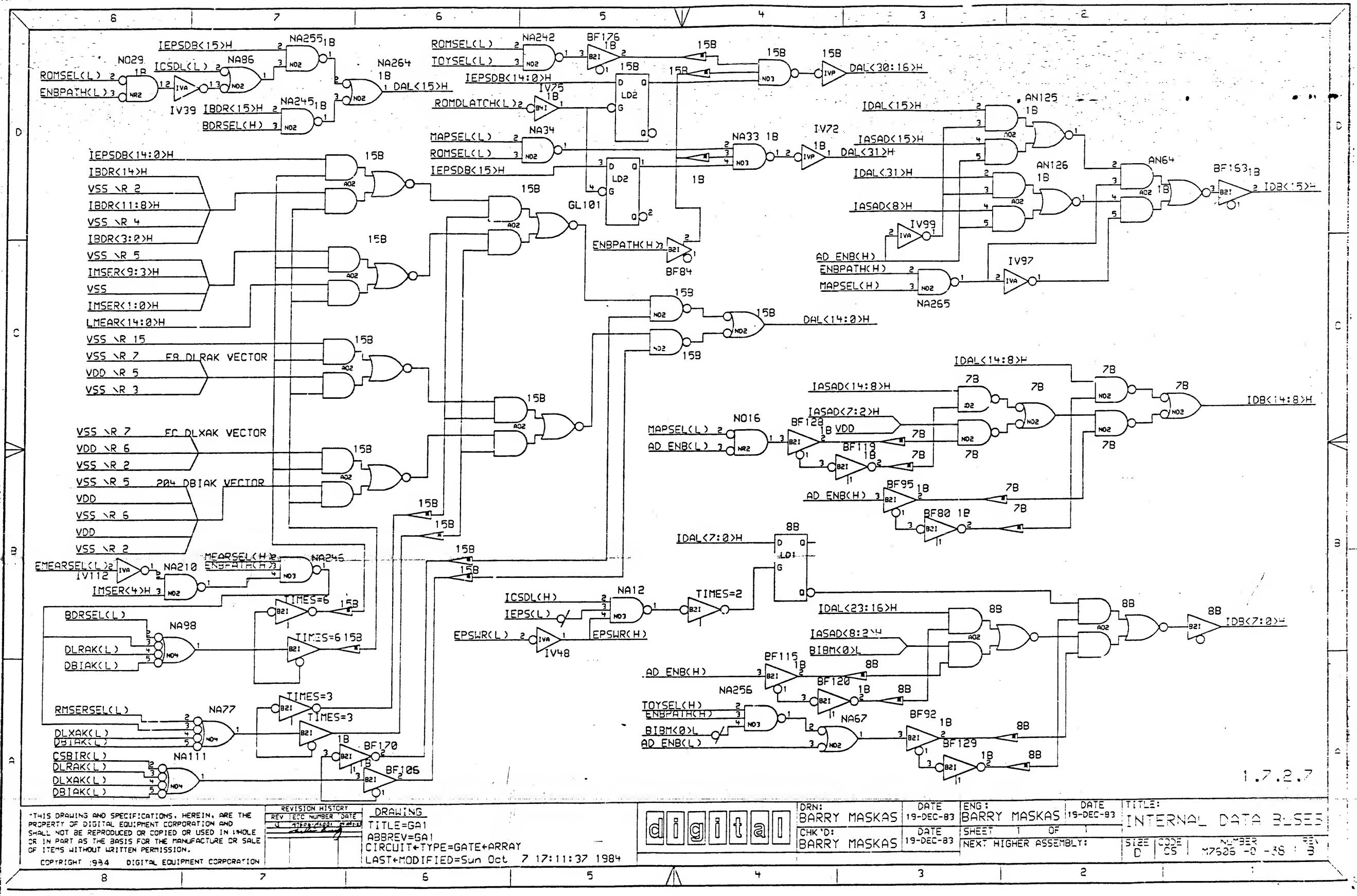
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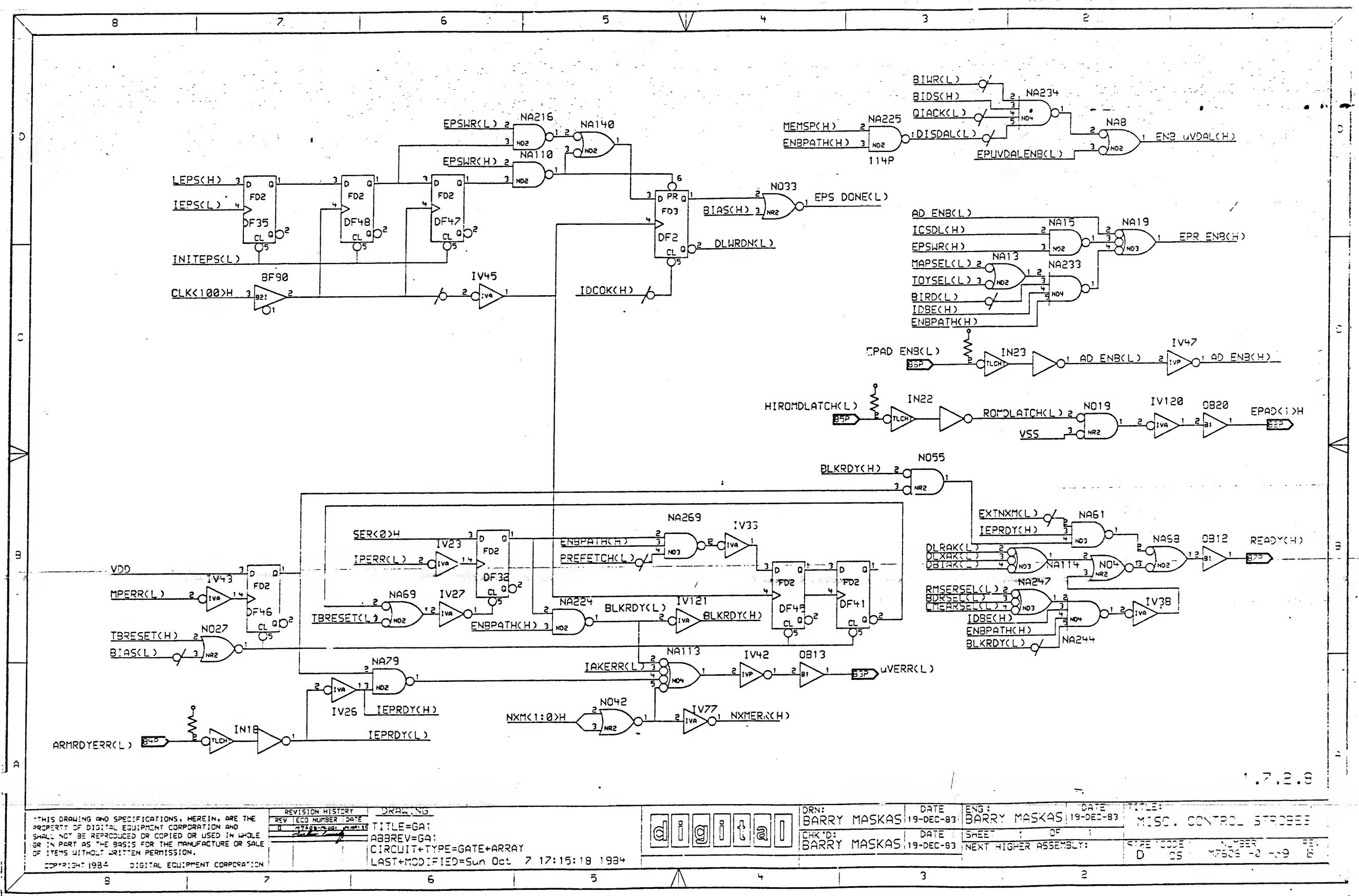
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REV EDITION NUMBER DATE			TITLE=GA1		CHK'D: BARRY MASKAS	DATE 18-DEC-83	SHEET 1 OF 1		
M7506-2-3-1 12/83			ABBREV=GA1				NEXT HIGHER ASSEMBLY:		
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			LAST MODIFIED=Sun Oct 7 16:40:03 1984						

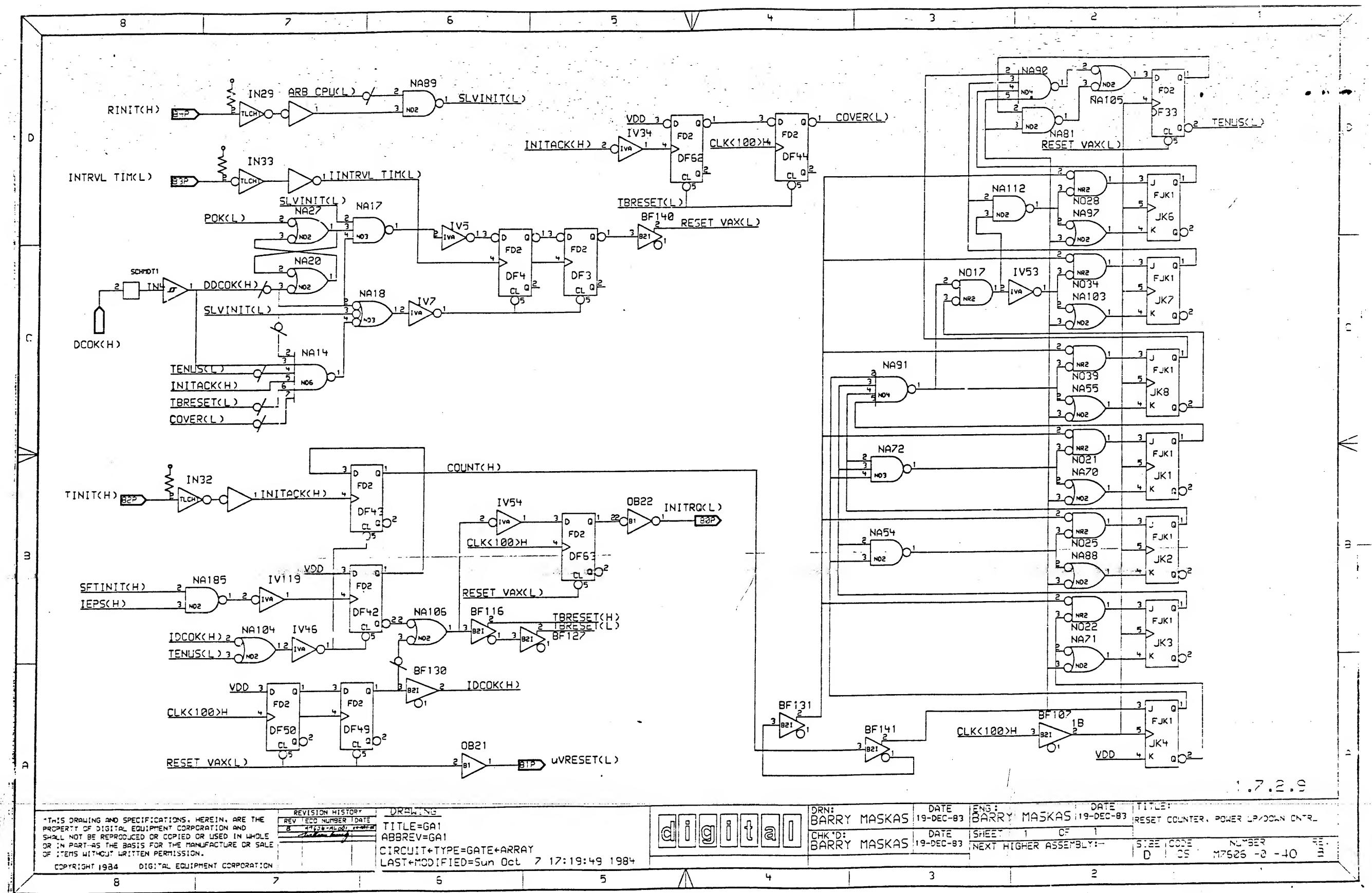


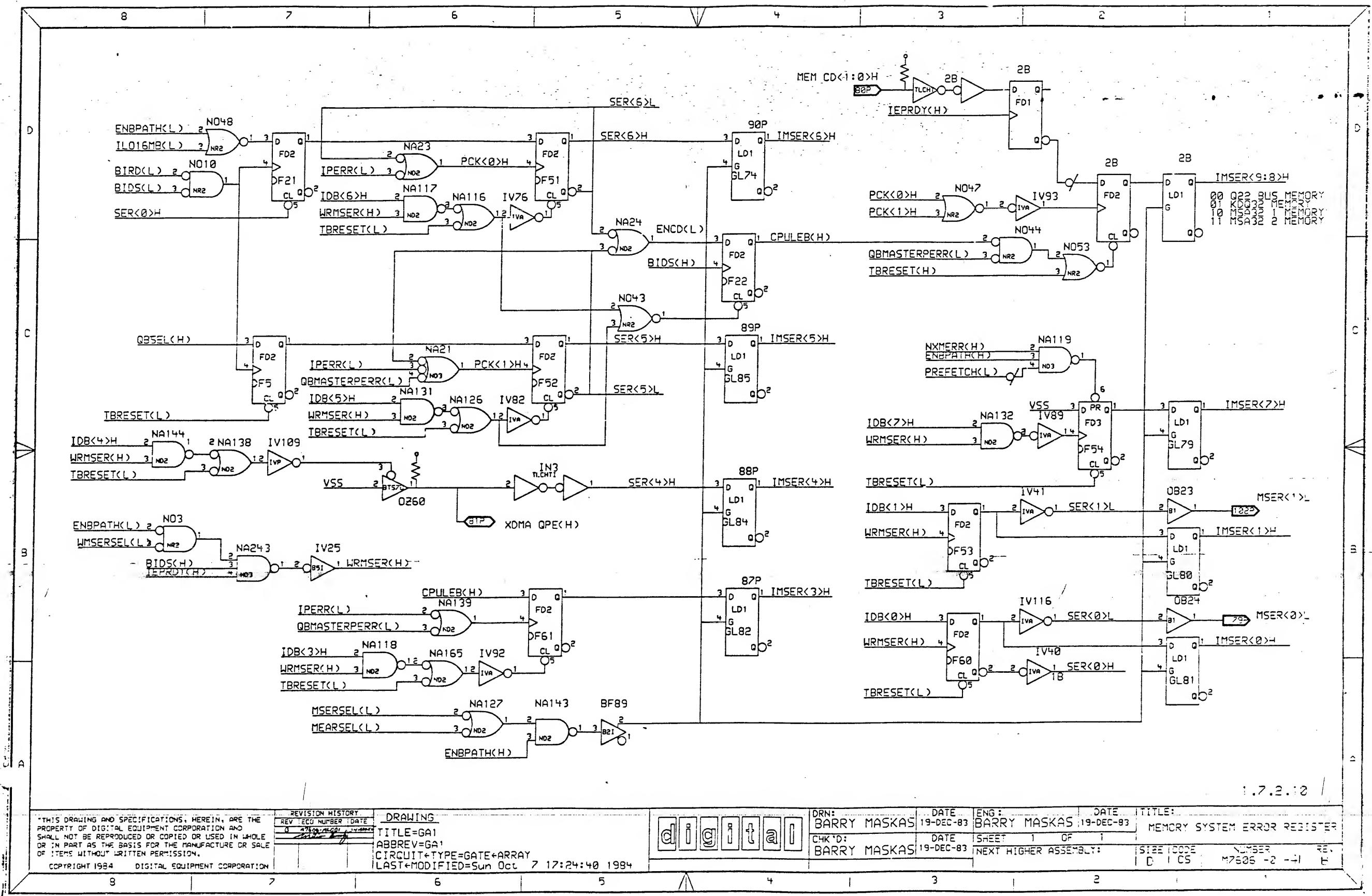


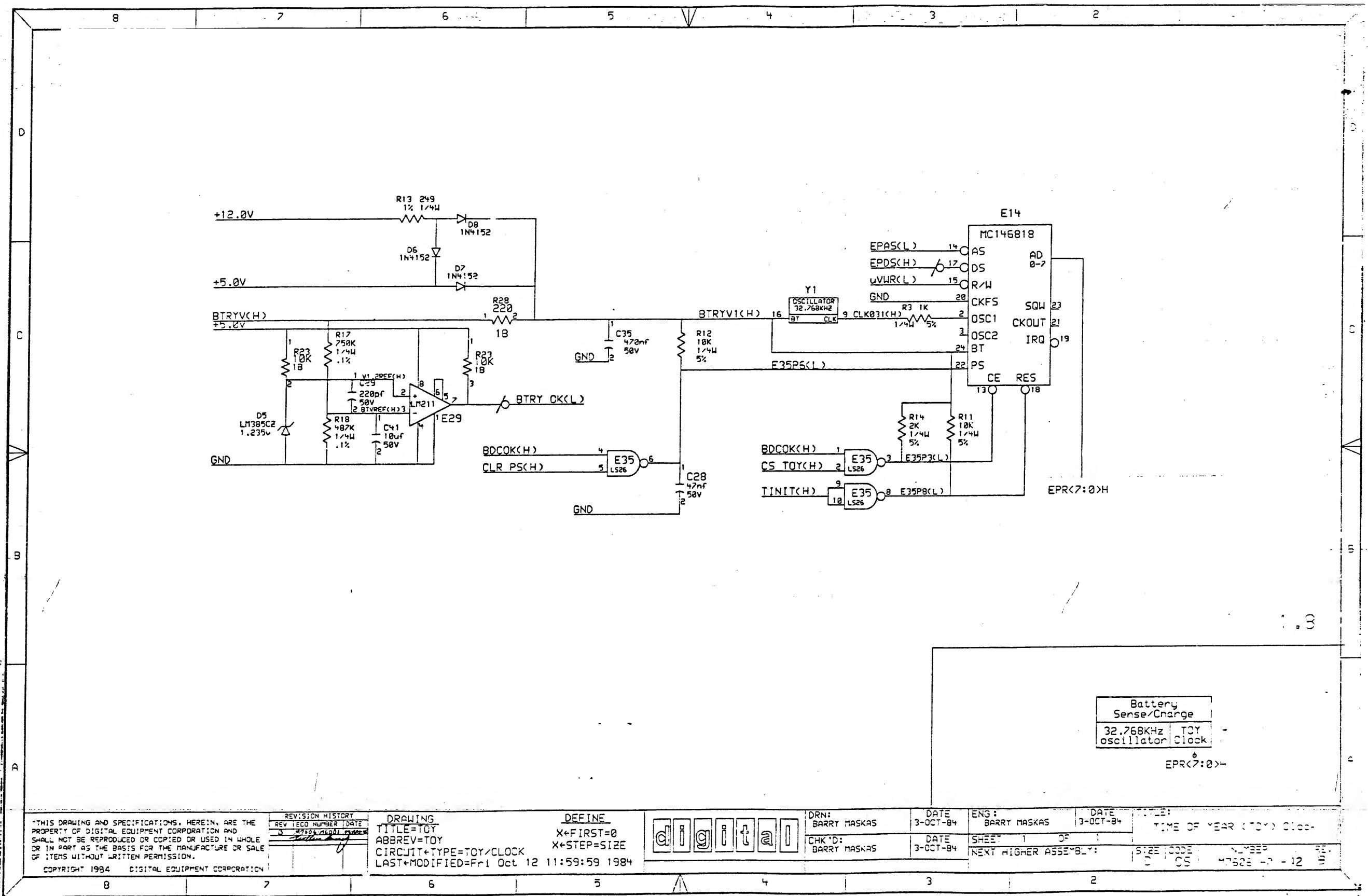


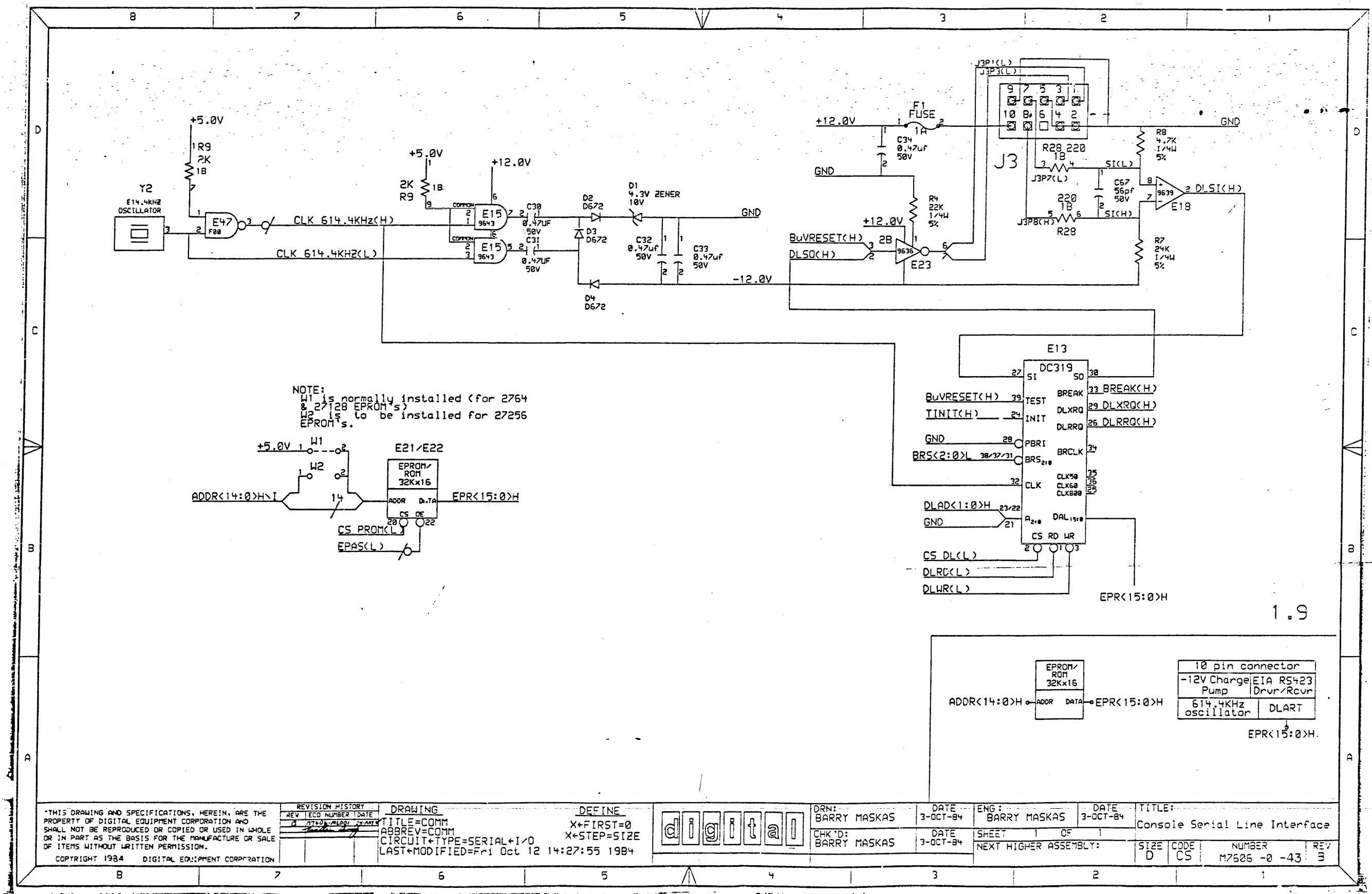


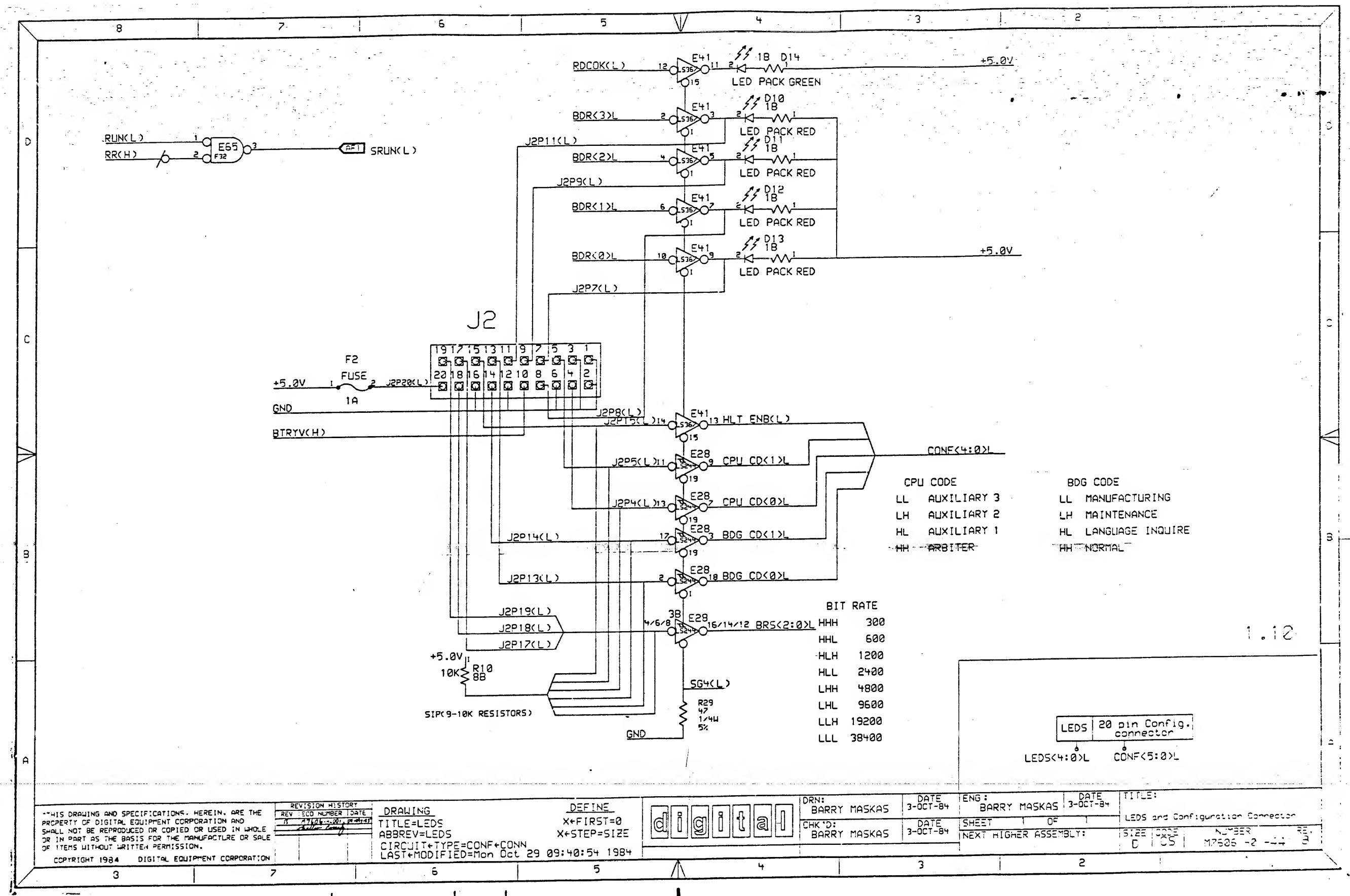


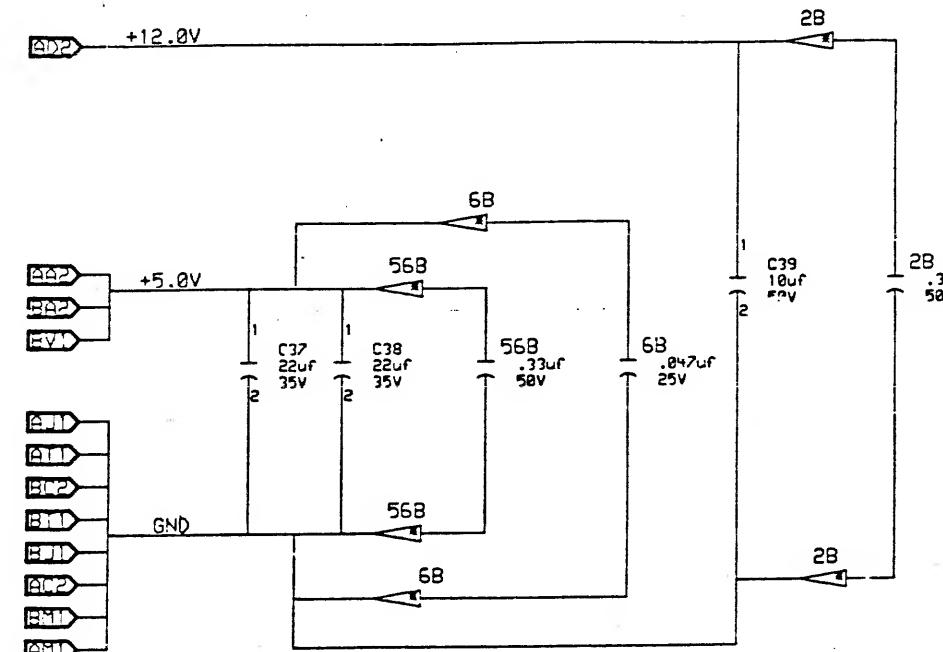












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REVISION HISTORY
REV ECO NUMBER DATE
B 19606-14001 07-1972

DR.DW

TITLE-KD01

LAST+MODIFIED=Sun Oct 7 20:49:41 198

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DRN:
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CHK 11
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~~ERRY MASKAS~~

DATE
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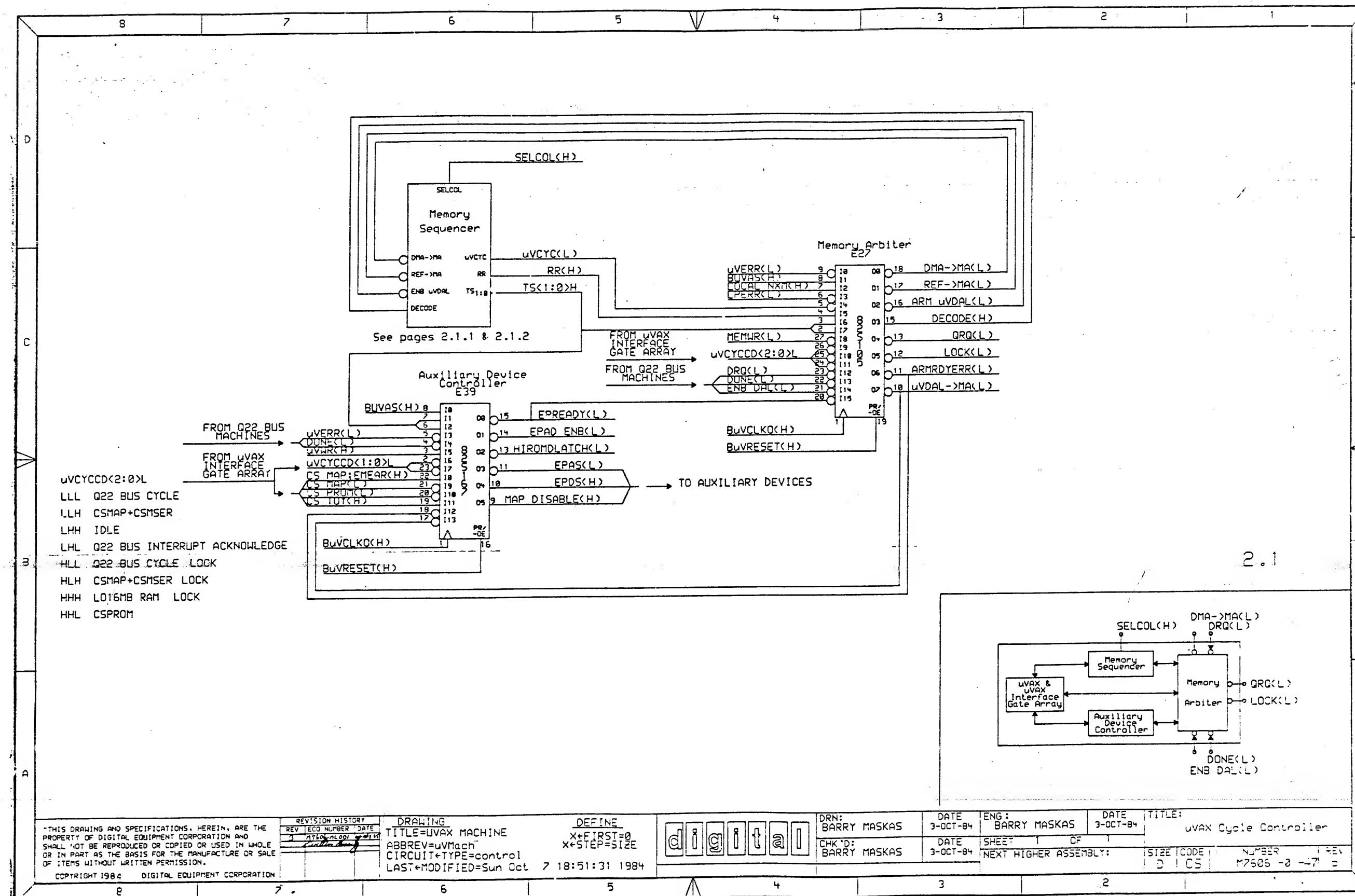
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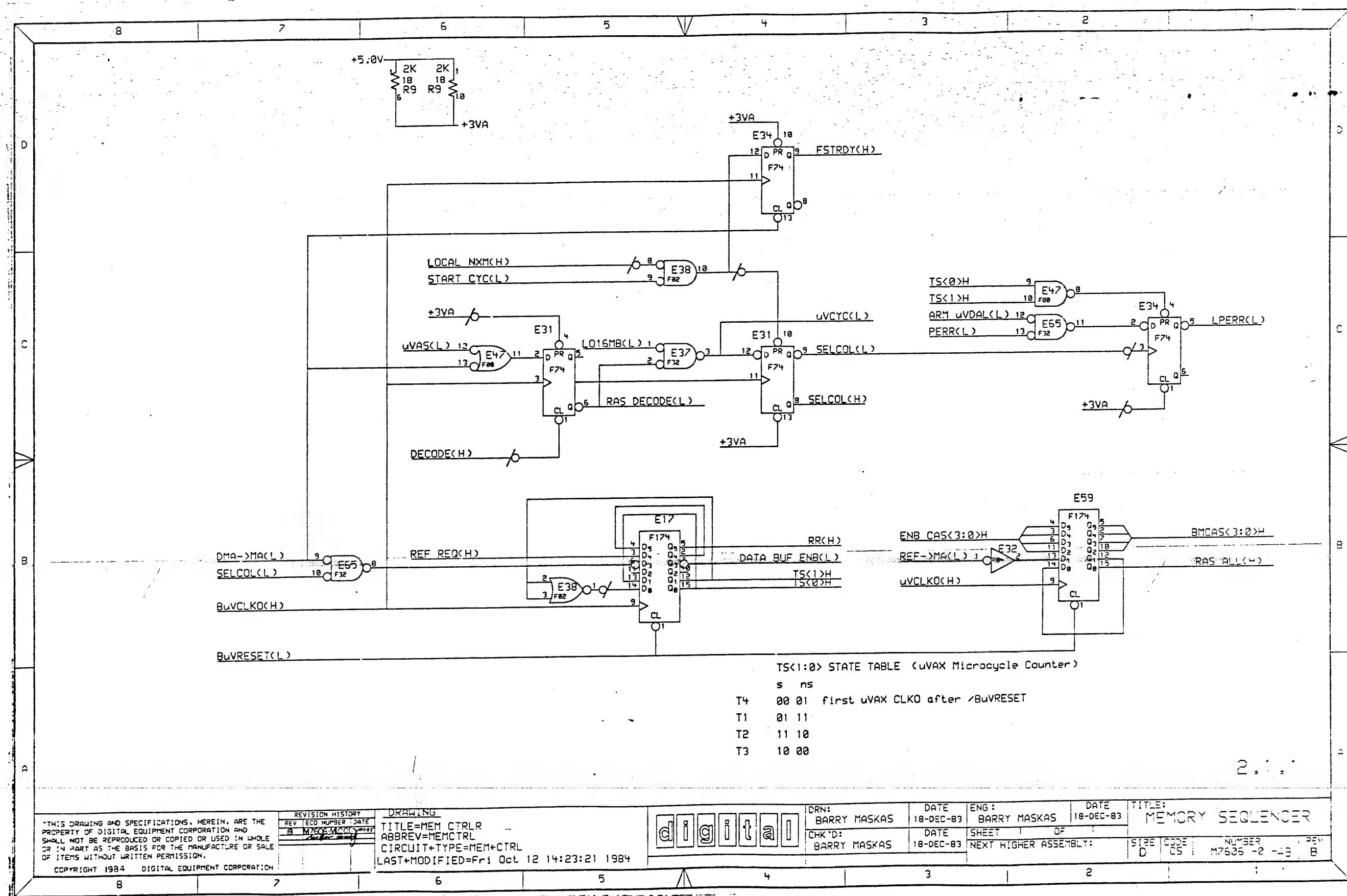
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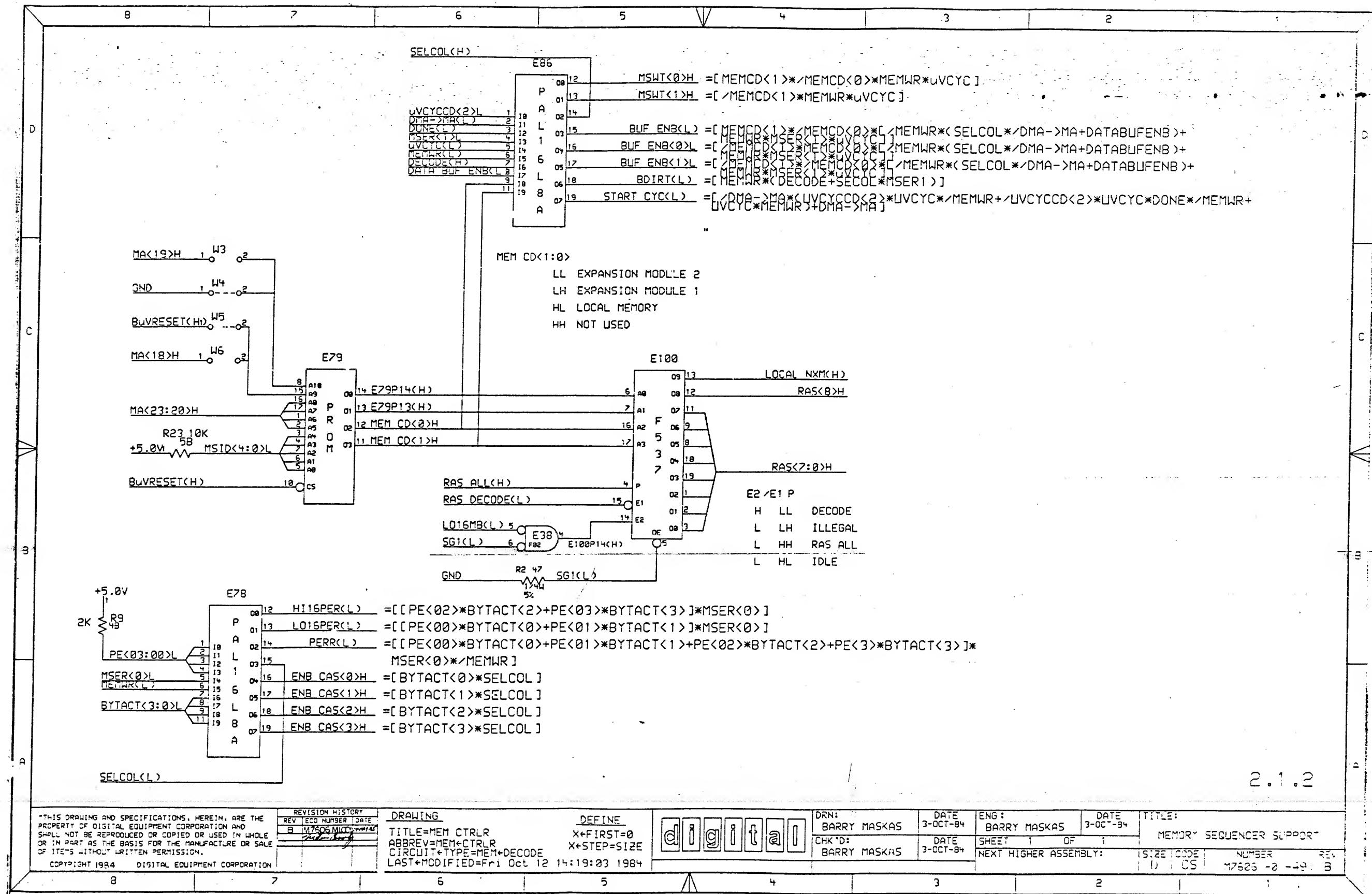
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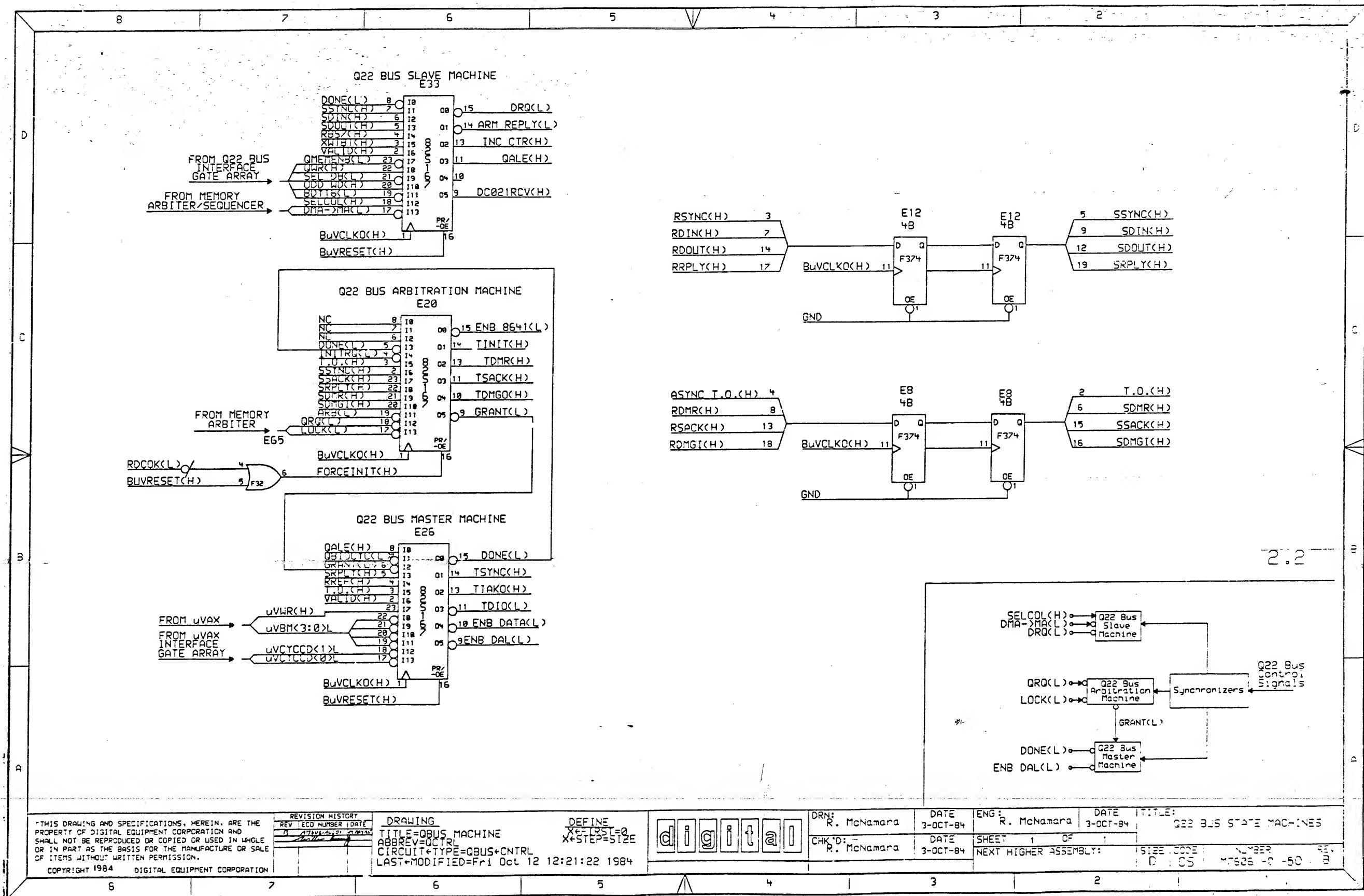
coupling C

Capacitors









NAME 23_053L1_00_E27 ;MEMORY ARBITER MACHINE
OPTION PRESET
INPUT -EPRDY, -ENBADR, -DONE, -DRQ, -CYCD0, -CYCD1, -CYCD2,
INPUT -MEMUR, S0, S1, RR, -VCYC, -LPERR, LOCALNMX, BVAS, -VERR
OUTPUT -DALMA, -RDYERR, -LOCK, -QRQ, DECODE, -ARMDAL, -REFMA, -DMAMA

LOCAL FLAG ;LOCK FLAG PREVENTS VAX FROM CHANGING MEMORY UNTIL Q22 BUS
;MASTERSHIP, Q22 BUS AND REFRESH CYCLES ARE ALLOWED.
MACHINE 23_053L1_00_E27

```

STATE POWERUP :LET REFRESH OR Q22 SLAVE THROUGH UNTIL Q22 BUS OWNED.
IF [ -DONE * SI * -S0 * RR ] THEN FINISHUP [ -DMAMA, -DALMA, -DECODE,&
-ARMDAL, -FLAG ]
IF [ -DONE * DRQ ] THEN FINISHUP [ -DMAMA, -DALMA, -DECODE,&
-ARMDAL, -FLAG ]
IF [ DONE * -ENBADR * CYCD0 ] THEN VXT12 [ RDYERR, ARMDAL ] ;LOCAL MISS.
IF [ DONE * ENBADR * CYCD0 ] THEN Q22MT3 [ -DALMA ] ;LOCAL MISS AND GLOBAL HI.
IF [ DONE * CYCD1 * -CYCD0 ] THEN VXT12 [ RDYERR ] ;FINISH UP THE MAP CYCLE.

```

STATE SYNCUP, NUMBER -LLLLLH
GOTO FINISHUP [-DMAMA, -DALMA, -DECODE, -ARMDAL]

```

STATE FINISHUP, NUMBER -HLLLH : Q22 SLAVE CYCLES HAVE TOP PRIORITY, REFRESH
IF [ -LPERR * DRQ ] THEN Q22SLAVE [ DMAMA ]
IF [ -LPERR < RR * -DRQ ] THEN REFRESH [ RFMMA ] ; LPERR IS FOR OPTIMIZATION
IF [ FLAG * -RR * -DRQ ] THEN VXT10 ; IF FLAGWAIT FOR DONE.
IF [ -S1 * -S0 * -EPRDY * -FLAG * -RR * -DRQ ] THEN VSCLAVE [ DALMA ]

```

STATE REFRESH, NUMBER -HHHL
GOTO RT2

STATE RT2, NUMBER -LLLLL
GOTO RT3

STATE RT2, NUMBER -LLLLL, RECALL, POSITIONAL AND LOCAL NAME(H) ASSERT

GOTO RT4

GOTO RT5 [-RDYERR]
STATE RT5
GOTO RT6 [-REFMA]

STATE RT6
GOTO SYNCUP [-DECODE, -RDYERR]

STATE Q22SLAVE, NUMBER -HLLLL ;LOCAL MEMORY IS SLAVE TO Q22 BUS MASTE
GOTO RT2 [DECODE]

STATE VXSLAVE, NUMBER -HHLLL ;LOCAL MEMORY IS SLAVE TO VXT3
GOTO VXT3 [DECODE]

```

STATE VXT3, NUMBER -LHLLL
IF [ S1 * -$0 * VCYC * BVAS * CYCD2 * -DONE ] THEN READY [ ARMDAL, RDYERR ]
IF [ S1 * -$0 * VCYC * BVAS * -CYCD2 * -CYCD1 * -CYCD0 * DONE ] THEN READY [ ARMDAL, RDYERR ]
IF [ S1 * -$0 * VCYC * CYCD1 * CYCD0 * DONE * EPRDY ] THEN READY [ ARMDAL, RDYERR ]
IF [ S1 * -$0 * -BVAS * -VCYC ] THEN FINISHUP [ -DMAAMA, -DALMA, & -DECODE, -ARMDAL ] ; IF NOTHING TO DO GO LOOK FOR REFRESH OR Q22 SLAVE.
IF [ S1 * -$0 * VCYC * BVAS * -CYCD2 * -DONE ] THEN RT4 [ QRQ, LOCK, FLAG ]
IF [ S1 * -$0 * -VCYC * BVAS ] THEN VXT41 [ -DECODE ] ; WHAT CYCLE TO DO?

```

```

STATE VXT41 ;FIND OUT WHAT KIND OF CYCLE TO RUN?
IF [ -VCYC * CYCD2 * -CYCD1 * CYCD0 ] THEN Q22CYC [ QRQ, -DALMA, ARMDAL ]
IF [ -VCYC * -CYCD2 * -CYCD1 * CYCD0 ] THEN PROMCYC [ RDYERR ]
IF [ -VCYC * -CYCD1 * -CYCD0 ] THEN RT4
IF [ -VCYC * CYCD2 * CYCD1 * -CYCD0 ] THEN Q22CYC
IF [ -VCYC * -CYCD2 * CYCD1 * -CYCD0 ] THEN Q22CYC [ LOCK ]
IF [ -VCYC * CYCD2 * CYCD1 * CYCD0 ] THEN Q22CYC [ ARMDAL ]
IF [ -VCYC * -CYCD2 * CYCD1 * CYCD0 ] THEN Q22CYC [ LOCK, ARMDAL ]

```

STATE READY ;CYCLE IS RUNNING AND EPR MACHINE ASSERTS EPRDY
IF [-S1 * S0] THEN VXT6 ;TO STROBE MEMCD<1:0> OR MSER WRITE DATA

STATE VXT6 ;IF VAX ERROR PIN IS ASSERTED, EXTRA uCYCLE OCCURS.
IF [VERR] THEN VXT9 [-LOCK, -QRQ] ;FREE Q22 BUS ON ERRORS OR MEMORY WRITES
IF [-VERR * -MEMWR] THEN VXT7 [-QRQ, -DECODE, -RDYERR, -FLAG]
IF [-VERR * -MEMWR] THEN VXT7 [-LOCK, -DECODE, -RDYERR, -FLAG, -OPA]

STATE VXT7, NUMBER -LLLHH
GOTO VXT8 [-DMA/MA. -DECODE. -DAI MA. -ARMDAI

```
STATE VXT8, NUMBER -HLLHH ;IF LOCAL PARITY ERROR THEN PROTECT MEMORY AND WAIT  
IF [ LPERR ] THEN VXTHOLD [ -LOCK ]  
IF [ -LPERR * -RR * -DRQ ] THEN VXSCLAVE [ DALMA ] ;ALLOW Q22 IAKS.  
IF [ -LPERR * RR * -DRQ ] THEN REFRESH [ REFMA ] ;ALLOW REFRESH.  
IF [ -LPERR * DPO ] THEN Q22SLAVE [ DMAMA ] ;ALLOW Q22 SLAVE.
```

STATE VXTHOLD ;FORCE VAX MACHINE CHECK, THEN ALLOW MEMORY CYCLES
IF [RVAS = \$1 * -50 * -VERR] THEN VXTH9

STATE VXT9 ;STALL ONE MICROCYCLE IF VAX SAW AN ERROR.
IF [\$1 == \$0 || \$1 == LOCALNM] THEN VXT2 [-DECODE, -RDYERR]
IF [\$1 == \$0 || LOCALNM] THEN RT3 [-DECODE, -GRQ, -RDYERR, -ARMDAL]

```

STATE VXT10 :STALL UNTIL Q22 BUS MASTERSHIP THEN RUN READ LOCK CYCLE.
IF [ S1 == -50 == DONE == BVAS == -CYCD2 == -CYCD1 == -CYCD0 ] THEN FINISHUP&
[-FLAG]
IF [ S1 == -50 == -DONE == BVAS == -CYCD2 == -CYCD1 == -CYCD0 ] THEN FINISHUP
IF [ S1 == -50 == -DONE == -BVAS ] THEN VXT8 [-FLAG, -DMAMA, -QRQ, -DALMA,&
-ARMDA ]

```

STATE PROMCYC ;EPR MACHINE RUNS A PROM CYCLE WHEN RDYERR IS ASSERTED.
IF [EPRDY] THEN RT4 ;EPR MACHINE ASSERTS EPRDY WHEN PROM CYCLE IS DONE.

STATE VXT12 ;EPR MACHINE IS DOING THE SYNCING.
IF [EPRDY] THEN READY [RDYERR] ;EPR MACHINE IS DONE AND VAX
;IS FINISHING.

STATE 022CTC ;G22 BUS DATA CYCLE OR IAK
IF [S1 * S0] THEN POWERUP [QRQ]

110

STATE Q22MT3 [GET IN STEP AND GO RUN THE MISS-HIT CYCLE, TELL EPR MACHINE.
IF I S1 * -S2] THEN Q22MT4 [DMAMA, RDYERR]

STATE Q22MT4, NUMBER -HHLLH
GOTO VMSL2MF

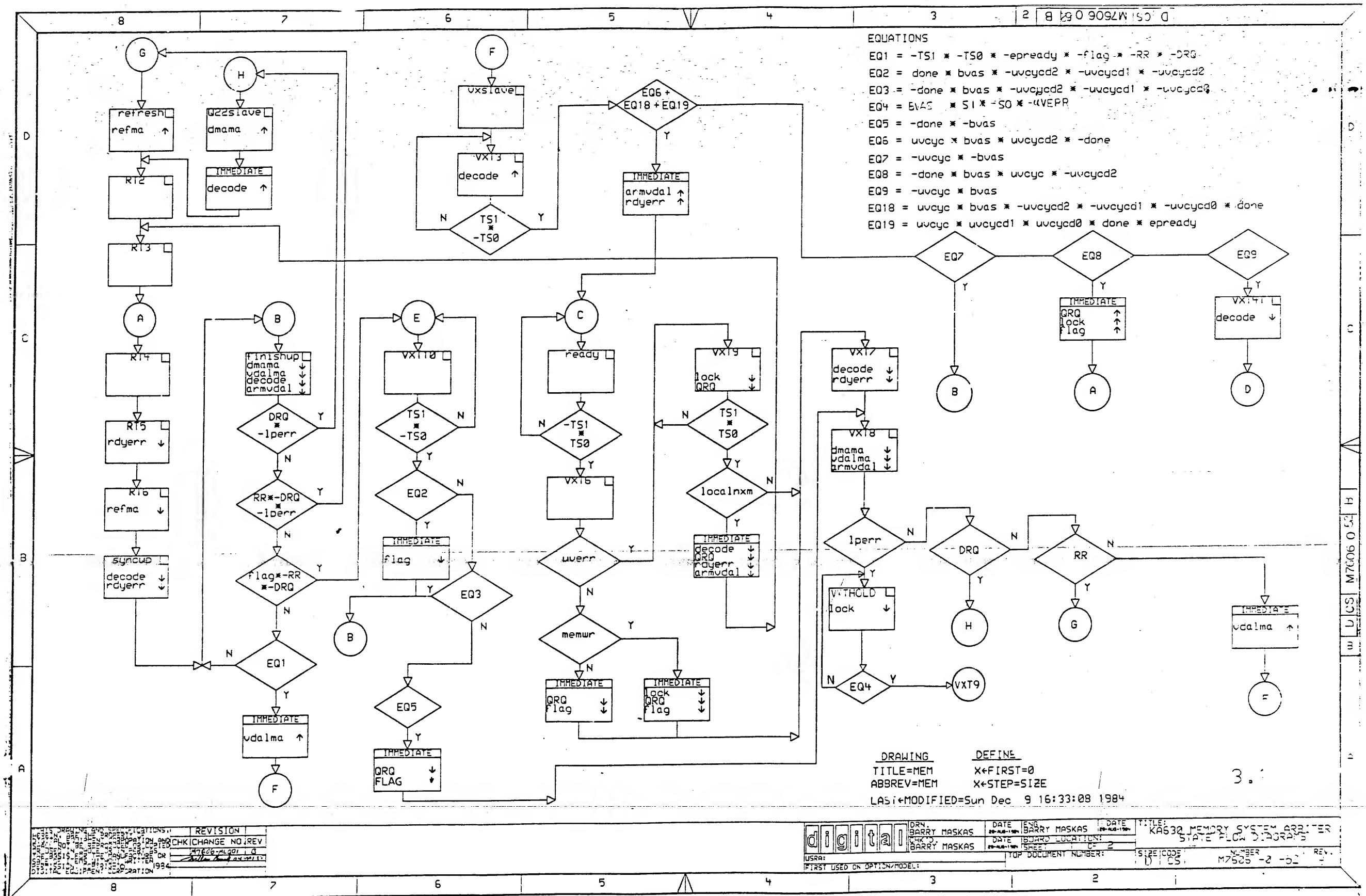
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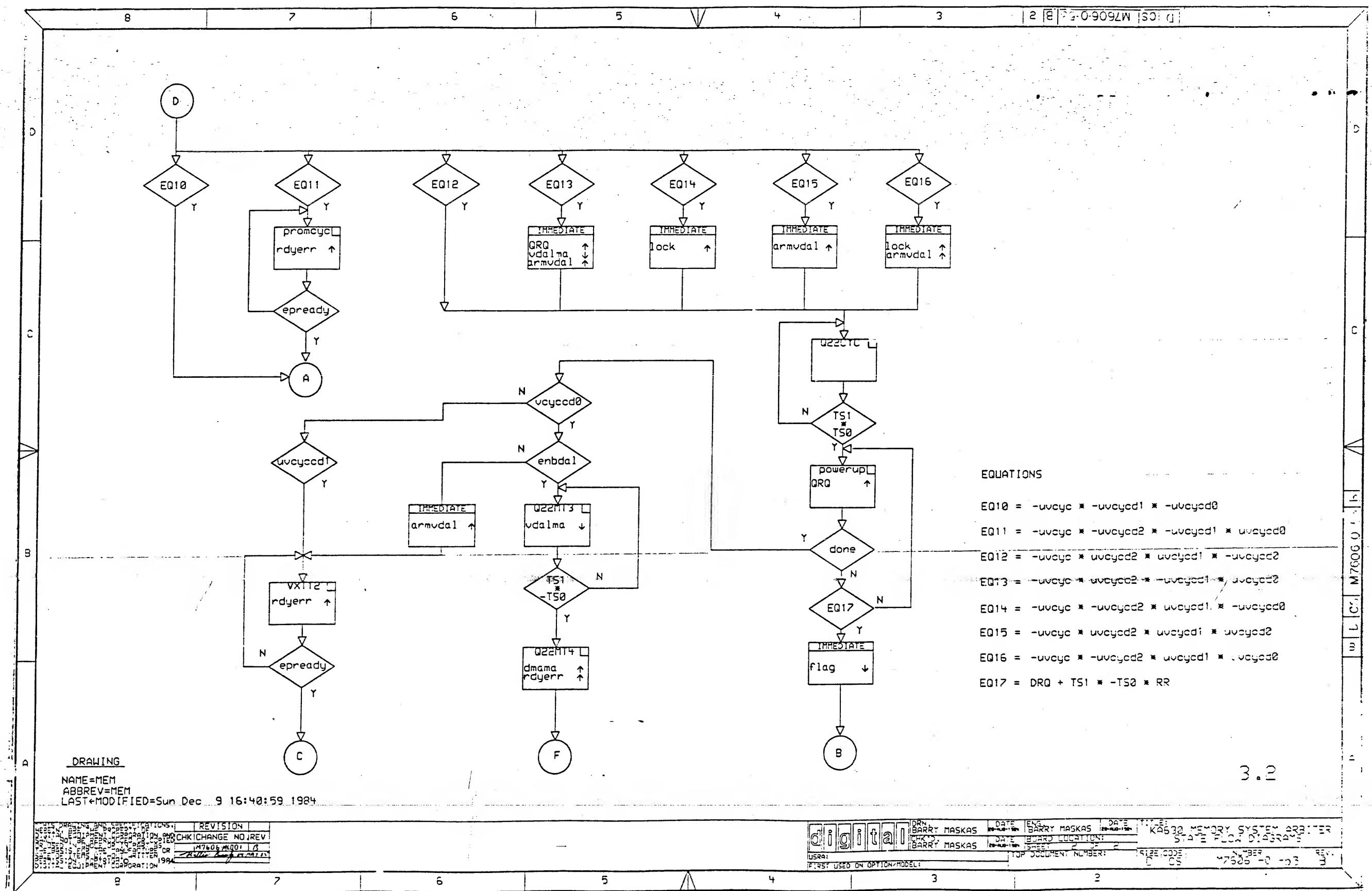
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DRW. *J. Donohy* DATE ENG. R. McNAMARA DATE T
 89-AUG-95 89-AUG-95
 CHK'D. DATE BOARD LOCATION: S
 R. McNAMARA 89-AUG-95 SHEET 1 OF 1
 [4,550] 09-AUG-95 07:40 NEXT HIGHER ASSEMBLY: S

**MEMORY ARBITER
LISTING**





D
NAME 23_014L3_00 ;KA630 LOCAL I/O CONTROL MACHINE revision 2
OPTION PRESET
INPUT NC1, -UVDALMA, -RDYERR, CSTOY, -CSPROM, -CSMAP, CSMAPEMEAR,
INPUT -UVCYC0, -UVCYC0, NC0, UVWR, -DONE, -UVERR, TS0, TS1, BUVAS
OUTPUT NC3, MAPDISABLE, EPDS, -EPAS, NC2, -HIROMDLATCH, -EPADENB, -EPREADY
MACHINE 23_014L3_00

STATE POWERUP
GOTO ST1 [-MAPDISABLE, -EPDS, -EPREADY, -EPAS, -HIROMDLATCH]

STATE ST1, NUMBER LLHLL
IF [TS1 * -TS0 * BUVAS * -UVERR] THEN ST2
IF [TS1 * -TS0 * UVERR] THEN EXTEND

STATE ST2, NUMBER LLLLH ;WHAT SHOULD RUN? IF Q22 BUS PUT ADDRESS ON EPR.
IF [-UVERR * RDYERR * -UVCYC0] THEN LOCALCYC [EPREADY]
IF [-UVERR * -UVCYC0 * -UVCYC0 * CSTOY] THEN TOFCYC [EPADENB]
IF [-UVERR * -UVCYC0 * -UVCYC0 * CSPROM] THEN PROMCYC
IF [-UVERR * UVCYC0 * UVCYC0 * CSMAP * CSMAPEMEAR] THEN MAPCYC [EPADENB]
IF [-UVERR * UVCYC0 * UVCYC0 * -CSMAP * -CSMAPEMEAR] THEN MSERWCYC
IF [-UVERR * -UVCYC0 * -UVCYC0 * -CSMAP * -CSMAPEMEAR] THEN EMEARCYC
IF [-UVERR * -UVCYC0 * -UVCYC0 * -CSTOY * -CSMAPEMEAR * -RDYERR * -TS1 * & .
-TS0] THEN AUTOCYC
IF [-UVERR * (-UVCYC0 * UVCYC0) + (-UVCYC0 * UVCYC0 * -CSPROM)] THEN &
Q22CYC [EPADENB]
IF [UVERR] THEN EXTEND

STATE EXTEND, NUMBER LLHLL
IF [TS1 * -TS0] THEN MS1

STATE LOCALCYC ;FAST READY FLEW BY BUT EPREADY ASSERTS TO STROBE ERRORS.
IF [-RDYERR * -UVDALMA] THEN ST1 [-EPREADY, -HIROMDLATCH, -EPAS]

STATE TOFCYC, NUMBER HLLHH ;TOY CLOCK CYCLE
GOTO TOYT0

STATE TOYT0, NUMBER HLLHL ;ADDRESS SETUP TIME
GOTO TOYT1 [-EPAS] ;CHIP SELECT AND ADDRESS ARE STABLE SO GO TO IT.

STATE TOYT1, NUMBER HLLHL
GOTO TOYT2 ;ADDRESS HOLD TIME.

STATE TOYT2, NUMBER HLLHL
GOTO TOYT3 [-EPADENB]

STATE TOYT3, NUMBER HLLLL
GOTO TOYT4 ;PREVENT TRISTATE OVERLAP.

STATE TOYT4, NUMBER HLHLL
GOTO TOYT5 [-EPDS] ;GET OR PUT THE DATA.

STATE TOYT5, NUMBER LLHLL ;DELAY FOR DATA ACCESS TIME.
IF [-TS1 * TS0] THEN TOYT6

STATE TOYT6, NUMBER LHLLL ;TELL UVAX THAT CYCLE CAN FINISH.
GOTO MS1 [EPREADY]

STATE PROMCYC ;PROM CYCLE
IF [UVDALMA * CSPROM * RDYERR] THEN PROMT1 [EPAS] ;ADDRESS OK?

STATE PROMT1 ;DELAY FOR ACCESS TIME.
IF [-TS1 * TS0] THEN PROMT2

STATE PROMT2 ;DELAY FOR ACCESS TIME, STROBE HI 16 BITS INTO LATCH.
GOTO PROMT3 [HIROMDLATCH] ;CHANGE ADDRESS TO LO 16 BITS.

STATE PROMT3 ;DELAY FOR ACCESS TIME.
IF [-TS1 * TS0] THEN PROMT4

STATE PROMT4, NUMBER HLLLL ;TELL MEMORY MACHINE AND UVAX TO FINISH.
GOTO MS1 [EPREADY]

STATE MAPCYC ;MAP CYCLE
IF [RDYERR * DONE * TS1 * TS0] THEN MAPT1 [-EPADENB] ;HAVE THE Q22 BUS?

STATE MAPT1, NUMBER LLLHH
GOTO MAPT2 ;PREVENT TRISTATE OVERLAP.

STATE MAPT2, NUMBER LLLHLH ;READ OR WRITE CYCLE?
IF [UVWR] THEN MAPT5 [MAPDISABLE] ;IF WRITE THEN Z THE MAP OUTPUTS.
IF [-UVWR] THEN MAPT3 [EPAS] ;IF READ THEN GET DATA ON EPR BUS.

STATE MAPT3, NUMBER HHLLH
GOTO MAPT4 ;DELAY ONE TICK TO SYNC UP.

STATE MAPT4, NUMBER HHLLL ;TELL UVAX AND MEMORY MACHINE TO FINISH.
GOTO MS1 [EPREADY]

STATE MAPT5
GOTO MAPT6 ;PREVENT TRISTATE OVERLAP.

STATE MAPT6 ;ENABLE THE WRITE DATA.
GOTO MAPT7 [-EPAS]

STATE MAPT7 ;ASSERT THE WRITE STROBE.
GOTO MAPT8 [-EPDS]

STATE MAPT8 ;SYNC UP WITH UVAX AND MEMORY MACHINE.
GOTO MSERWCYC [-EPADENB]

STATE MSERWCYC ;MSER WRITE CYCLE, GET THE Q22 BUS, STROBE THE DATA.
IF [RDYERR * DONE * TS1 * TS0] THEN MS1 [EPREADY]

STATE MS1, NUMBER LLLLH ;STROBE THE MSER DATA WITH EPREADY.
IF [TS1 * TS0] THEN MS2 [-EPREADY]

STATE MS2
GOTO POWERUP [-EPDS]

STATE EMEARCYC, NUMBER HHHHLH ;EXTERNAL MEAR CYCLE.
GOTO EM1

STATE EM1, NUMBER HHHLLH ;ENABLE THE EPR DATA AND TELL UVAX TO FINISH.
GOTO EM2 [-EPAS, EPREADY]

STATE EM2, NUMBER HHHLL
GOTO MS1 [-EPREADY]

STATE AUTOCYC ;NOTHING TO DO SO BACK FOR ANOTHER LOOK.
GOTO ST1 [-EPREADY, -HIROMDLATCH, -EPAS, -EPADENB]

STATE Q22CYC ;Q22 BUS IAK OR Q22 BUS READ OR WRITE.
IF [RDYERR] THEN Q22T1 [-EPADENB]

STATE Q22T1
IF [RDYERR * DONE * TS1 * TS0] THEN Q22T2 [EPREADY]

STATE Q22T2 ;WAIT UNTIL MEMORY MACHINE IS DONE.
IF [-RDYERR] THEN ST1 [-EPREADY, -HIROMDLATCH, -EPAS]

END

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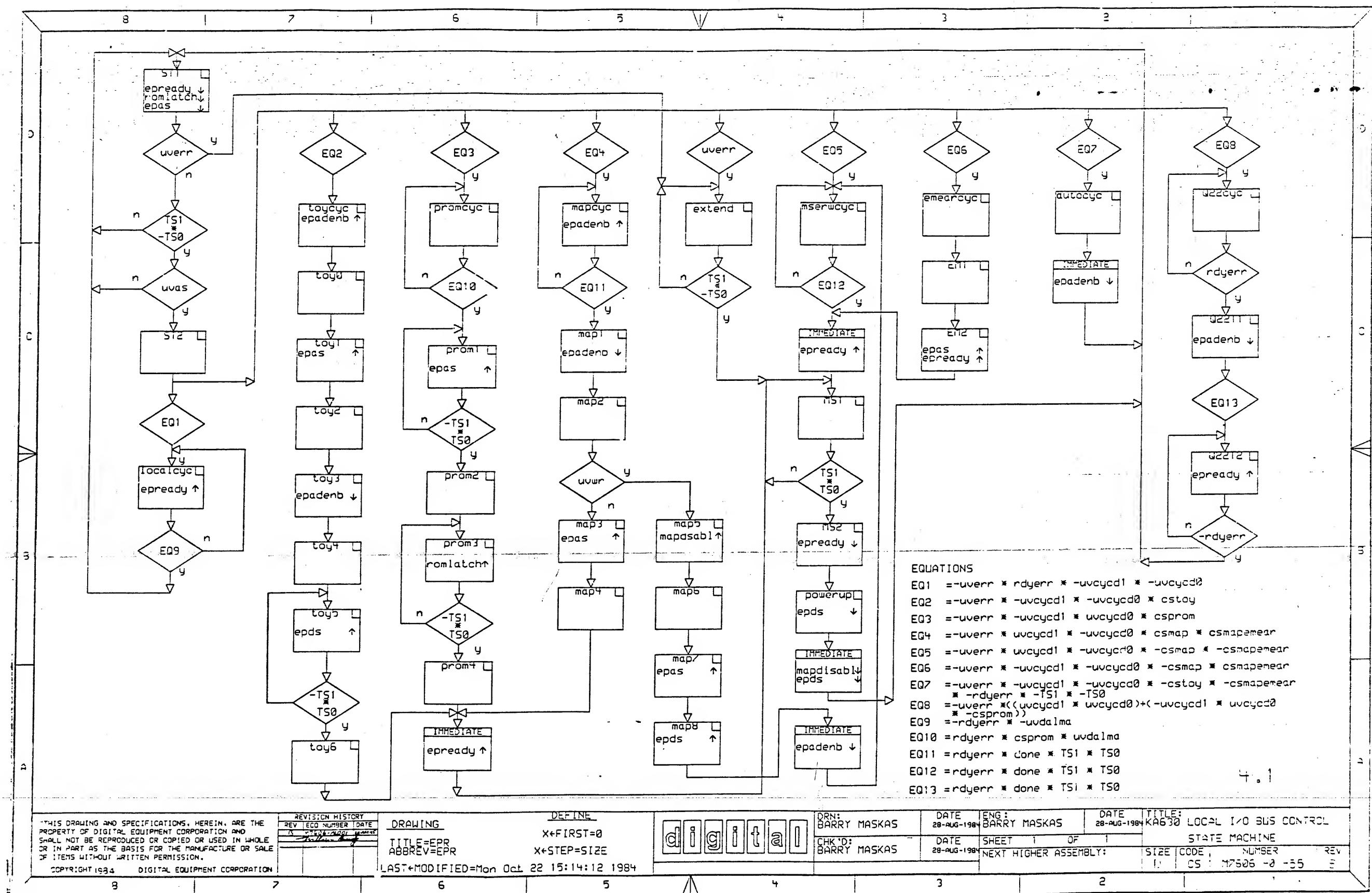
REVISIONS

CHK

CHANGE NO.

REV.

Drw. 7/20/85 Date 09-AUG-85 ENG. R. McNAMARA DATE 09-AUG-85 TITLE: LOCAL I/O CONTROL
MCNAMARA CHK'D. R. McNamara DATE BOARD LOCATION:
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FIRST USED ON OPTION/MODEL: SIZE CODE NUMBER REV.
D CS M7606-0-54 A



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1

S15 CS M7506-0-56
SIZE CODE NUMBER REV.
D 320E A

```

name 23_008L3_00_E20 ;Q22 bus arbitration control machine
input nci15, -lock, -qrq, -arb, sdmgi, sdmr, srply, ssack,
input ssync, nc16, t_o, -initrq, -done, nc12, nc11, nc10
output nco7, -grant, tdmgo, tsack, nc13, tdmr, tinit, -enb8641
machine q_bus_arb
state A
goto Q [-grant, -tdmgo, -tsack, -tdmr, tinit, -enb8641]
state B
if [-ssack * (arb + (-arb * sdmgi)) * (qrq + initrq) * (ssync + srply)] then E
if [-ssack * arb * qrq * -initrq * -ssync * -srply] then E [grant, -tdmr]
if [-ssack * arb * -qrq * -initrq * -ssync * -srply] then Q [tinit, -tdmr]
if [-ssack * (arb * sdmr) + (-arb * sdmgi)) * -qrq * -initrq] then C [tdmgo]
if [-ssack * -arb * sdmgi * qrq * -initrq * -ssync * -srply] then E &
[grant, -tdmr, tsack]
if [-ssack * -arb * sdmgi * -initrq * -ssync * -srply] then Q &
[tinit, -tdmr, tsack]
if [ssack * (qrq + initrq) + -arb * -sdmgi * (qrq + initrq)] then [tdmr]
if [ssack * -qrq * -initrq + -arb * -sdmgi * -qrq * -initrq + &
arb * -qrq * -initrq * -sdmr] then [-tdmr]
state C
if [arb * ssack] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
if [arb * -ssack * t_o] then F [-tdmgo]
if [-arb * -sdmgi] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
state D
if [-ssync * -srply * arb * qrq * -initrq] then E [grant, -tdmr]
if [-ssync * -srply * arb * -qrq * -initrq] then E [-grant, -tdmr]
if [-ssync * -srply * arb * -initrq] then Q [tinit, -tdmr]
if [-ssync * -srply * -arb * qrq * -initrq] then E [grant, tsack, -tdmr]
if [-ssync * -srply * -arb * -qrq * -initrq] then E [-grant, tsack, -tdmr]
if [-ssync * -srply * -arb * initrq] then Q [tinit, tsack, -tdmr]
state E
if [-qrq * -lock] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
if [-qrq] then [-grant]
if [qrq] then [grant]
state F
goto H
state G
goto J
state H
goto K
state I
goto L
state J
goto K
state K
goto L
state L
goto M
state M
goto N
state N
goto P
state O
goto B [-tdmgo, -tsack, -tinit, -grant, enb8641]
state P
if [-initrq] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
state Q
if [-initrq] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
END

```

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REVISIONS
 CHK CHANGE NO. REV

DRW. *R. McNamara* DATE 09-AUG-85 ENG. R. MCNAMARA DATE 09-AUG-85
 CHK'D. *R. McNamara* DATE 09-AUG-85 BOARD LOCATION 1 OF 1
 DSK:5.72PC4.5501 09-AUG-85 SHEET 1 OF 1
 FIRST USED ON OPTION/MODEL: TITLE: Q22 BUS ARB. CTL
 MACHINE LISTING
 SIZE CODE NUMBER REV.
 D CS M7506-0-56 A

8

7

6

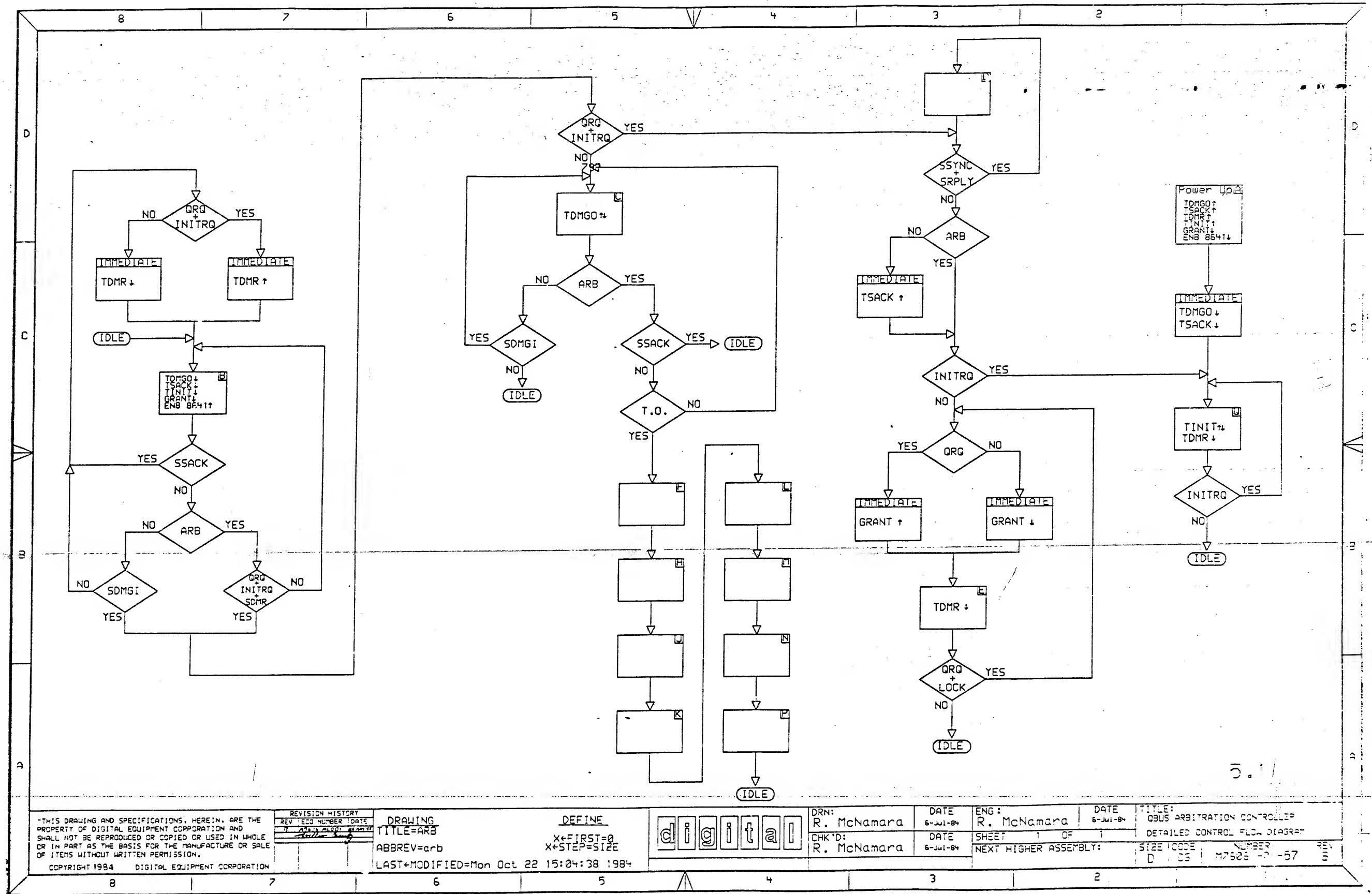
5

4

3

2

1



8 7 6 5 V 4 3 2 A CS M7606-0-58 REV. A SIZE CODE NUMBER

```

D
name 23_009L3_00_E26 ;Q22 bus master cycle control machine
input nci15, -cd0, -cd1, -bm0, -bm1, -bm2, -bm3, uVWR
input valid, nci16, t_o, rref, srply, -grant, -qbiocyc, qale
output nco7, -EnbDal, -EnbData, -tdio, nco3, tiako, tsync, -done
local first

machine q_bus_master
state A, number -hhhhh
if [-grant] then B [first, -EnbDal, -EnbData, -done, -tdio, -tiako, -tsync]
state B, number -hhhh1
if [grant * qale * -(-cd1)] then P [EnbDal]
if [grant * qale * (-cd1 * -cd0)] then T
if [grant * qale * (-cd1 * cd0)] then C [tdio, -first]
state C, number -h1hh1
goto D
state D, number -111h1
gotc E
state E, number -h1hhh
goto F
state F, number -111hh
goto H
state H, number -1hh1h
goto J [tiako]
state J, number -1hhhh
goto V
state K, number -1hh1h
goto L
state L, number -hh1hh
goto M
state M, number -1hh1h
goto N [-EnbData, -tdio, -first]
state N, number -1hh1h
if [-srply] then P [EnbDal, -tsync]
state P, number -h1hh1
goto R
state R, number -11hh1
goto S
state S, number -h1hhhh
goto T

state T, number -11hhh
if [qale * (-cd0 + (valid * qbiocyc))] &
then AP [-done]
if [qale * -cd0 * (-valid + qbiocyc)] &
then U [-tsync]
if [qale * cd0 * valid * -qbiocyc * -first] then [-tsync]
if [qale * cd0 * valid * -qbiocyc * first] then [tsync, -first]
state U, number -h1h11
goto V
state V, number -11h11
if [uVWR] then AB [EnbData]
if [-uVWR] then AJ [tdio, -EnbDal]
state AJ, number -hh1h1
if [t_o + srply] then AK
state AK, number -h11h1
goto AL
state AL, number -111h1
goto AM
if [-t_o] then [EnbData]
state AM, number -h111h
if [-t_o * -uVWR * (bm2*bm1) * first * -rref] then N &
[-EnbData, -tdio, -tiako, -first]
if [t_o + uVWR + -(bm2*bm1) + -first + rref] then AN &
[-EnbData, -tdio, -tiako]
state AN, number -1111h
if [-srply * -t_o * first * (bm2*bm1) * -uVWR] &
then V [-first]
if [-srply * -t_o * first * (bm2*bm1) * uVWR] &
then AB [-first, EnbData]
if [-srply * (t_o + -bm2*bm1) + -first] &
then AP [-tsync, done, -EnbDal]
state AP, number -hh1hh
if [grant * -qbiocyc * -qale] then S
if [-grant + qbiocyc + qale] then A
state AB, number -hh1hh
goto AC
state AC, number -1hh1h
goto AD
state AD, number -hhhhh
goto AE [tdio]
state AE, number -hhhh1h
if [t_o + srply] then AF
state AF, number -h1hh1h
if &
[-t_o * first * (bm2*bm1) * -(<-uVWR + bm0 * bm3) * rref] &
then K [-tdio]
if &
[t_o + -first + -(bm2*bm1) + rref * (-uVWR + bm0 * bm3)] &
then AH [-tdio]
state AH, number -11hh1h
goto AL
END

```

SIZE CODE NUMBER
A D 17686-0-58

B

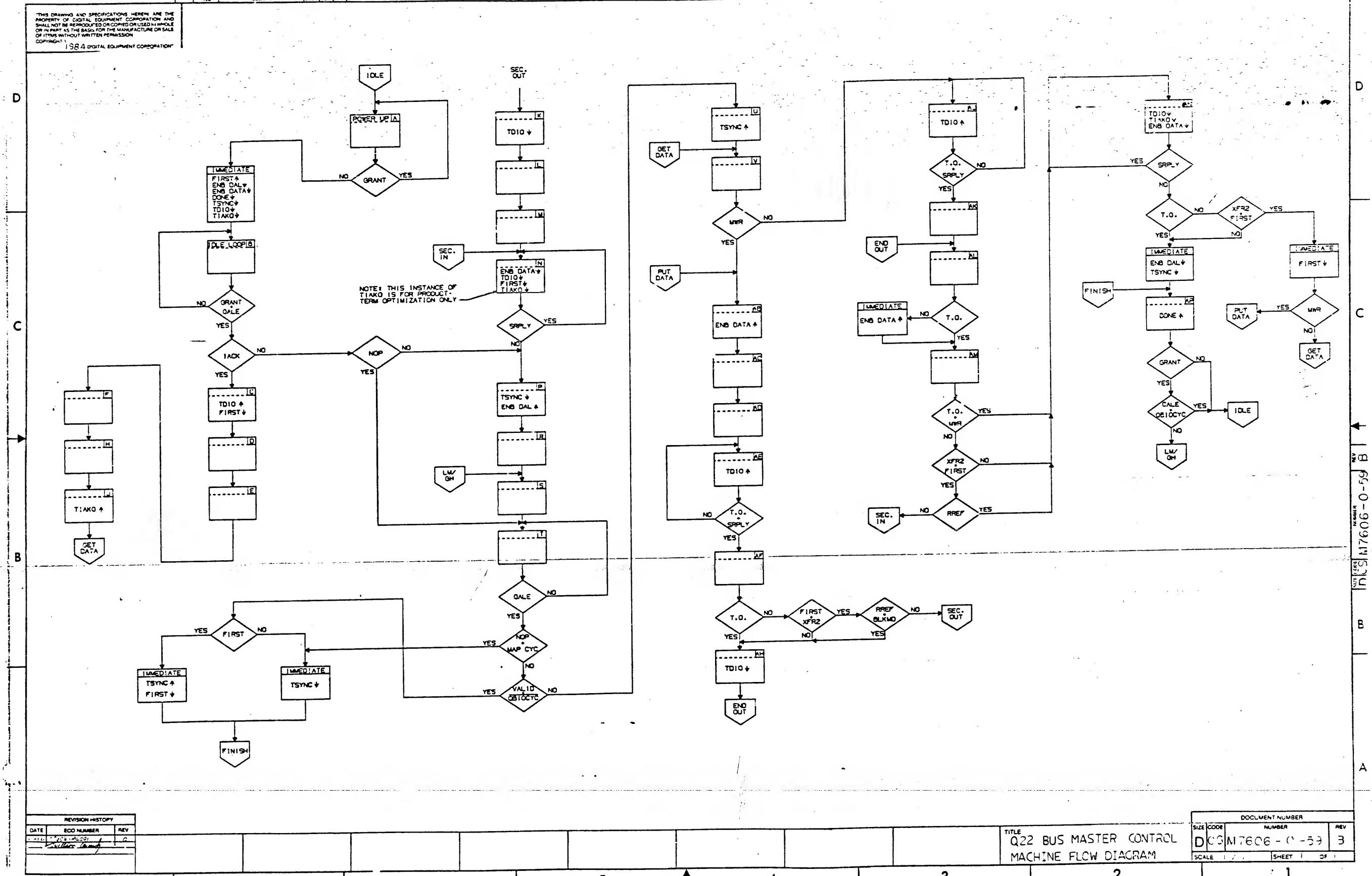
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REVISIONS
CHK CHANGE NO. REV

DRW. <i>J. J. J.</i>	DATE 09-AUG-85	ENG. R. McNAMARA	DATE 09-AUG-85	TITLE: Q22 BUS MASTER CTL MACHINE LISTING		
CHK'D R. McNAMARA	DATE 09-AUG-85	BOARD LOCATION: SHEET 1 OF 1				
DSK:6.T2PC4,5581 09-AUG-85 07:39			NEXT HIGHER ASSEMBLY:	SIZE D	CODE CS	NUMBER M7606-0-58
FIRST USED ON OPTION/MODEL:						REV. A

8 7 6 5 V 4 3 2 A CS M7606-0-58 REV. A SIZE CODE NUMBER



```

D
name 22_010L3_00_E33 ;Q22 bus slave cycle control machine
input -drq, -dmaMA, selcol, -bdy16, oddwd, -sel_db, qwr, -QMemEnb
input valid, nc16, xwtbt, rbs7, sduit, sdin, ssync, -done
output nco7, DC021rcv, nco5, qale, nco3, incctr, -armreply, -drq
local flag
machine q_bus_slave
state AA, number -hhhhh
goto A [DC021rcv, -drq, qale, -armreply, -flag]
state A, number -11111
if [-dmaMA] then A2 [qale]
state A2, number -1h111
goto B [-incctr]
state B1, number -1hh11
goto C [-armreply]
state C, number -11h11
always [-armreply]
if [-ssync * flag] then K [drq]
if [-ssync * -flag] then A &
    [DC021rcv, -armreply, -flag, -drq]
if [ssync * sduit * -dmaMA * -xwtbt * -bdy16 * -oddwd] then D [incctr, flag]
if [ssync * sduit * -dmaMA * (xwtbt + bdy16)] then E [drq, flag, incctr]
if [ssync * sduit * -dmaMA * -xwtbt * -bdy16 * oddwd] then E &
    [drq, -flag, incctr]
state D
if [-sduit] then B1 [-incctr]
state E, number -11h1h
always [-armreply]
if [dmaMA] then [-drq]
if [-sduit] then J
if [sduit * dmaMA * selcol] then F
state F
if [-sduit] then H [-incctr]
state H, number -h1hh1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * -flag] then C [-armreply]
state J, number -h1hh1
if [dmaMA] then [-drq]
if [-ssync] then K
if [ssync * dmaMA * selcol] then J1
state J1, number -hh11h
goto H [-incctr]
state K, number -1111h
if [dmaMA + -drq] then A [DC021rcv, -armreply, -flag, -drq]
state L1, number -1hhhh
goto M [-armreply]

D
state M, number -11hhh
always [-armreply]
if [-sdin * -sduit] then N [DC021rcv]
state N, number -111h1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdin * -flag] then L1 [-DC021rcv, flag]
if [ssync * -(sdin * -flag) * sduit] then M [-armreply, flag]
state P, number -h1111
if [dmaMA] then [-drq]
if [-ssync] then K
if [ssync * dmaMA * selcol] then R
state R, number -hh111
goto R1 [-incctr]
state R1, number -hh1h1
goto R2 [-DC021rcv]
state R2, number -1hh1h
goto S [-armreply]
state S, number -11hh1
always [-armreply]
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdin * bdy16] then U
if [ssync * sdin * -bdy16] then T [incctr]
state T
if [-sdin * -rbs7] then V &
    [-incctr, DC021rcv, qale]
if [-sdin * rbs7 * oddwd] then S &
    [-incctr, -armreply]
if [-sdin * rbs7 * -oddwd] then P &
    [-incctr, DC021rcv, drq]
state U
if [-sdin] then V [DC021rcv, qale]
state V, number -h11h1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sduit] then V1 [-qale]
state V1, number -1hh1h
goto E [-armreply, flag, drq]
state B, number -1hh1h
if [-done * ssync * -sel_db * -QMemEnb] then B1A
if [-done * ssync * -sel_db * -QMemEnb] then H [flag, -incctr]
if [-done * ssync * sel_db] then N [-qale, DC021rcv]
if [done * dmaMA] then AA [-qale]
state B1A
if [-valid] then H [flag, -incctr]
if [valid * -qwr] then P [-qale, drq]
if [valid * qwr] then B1 [-qale, -incctr]
END

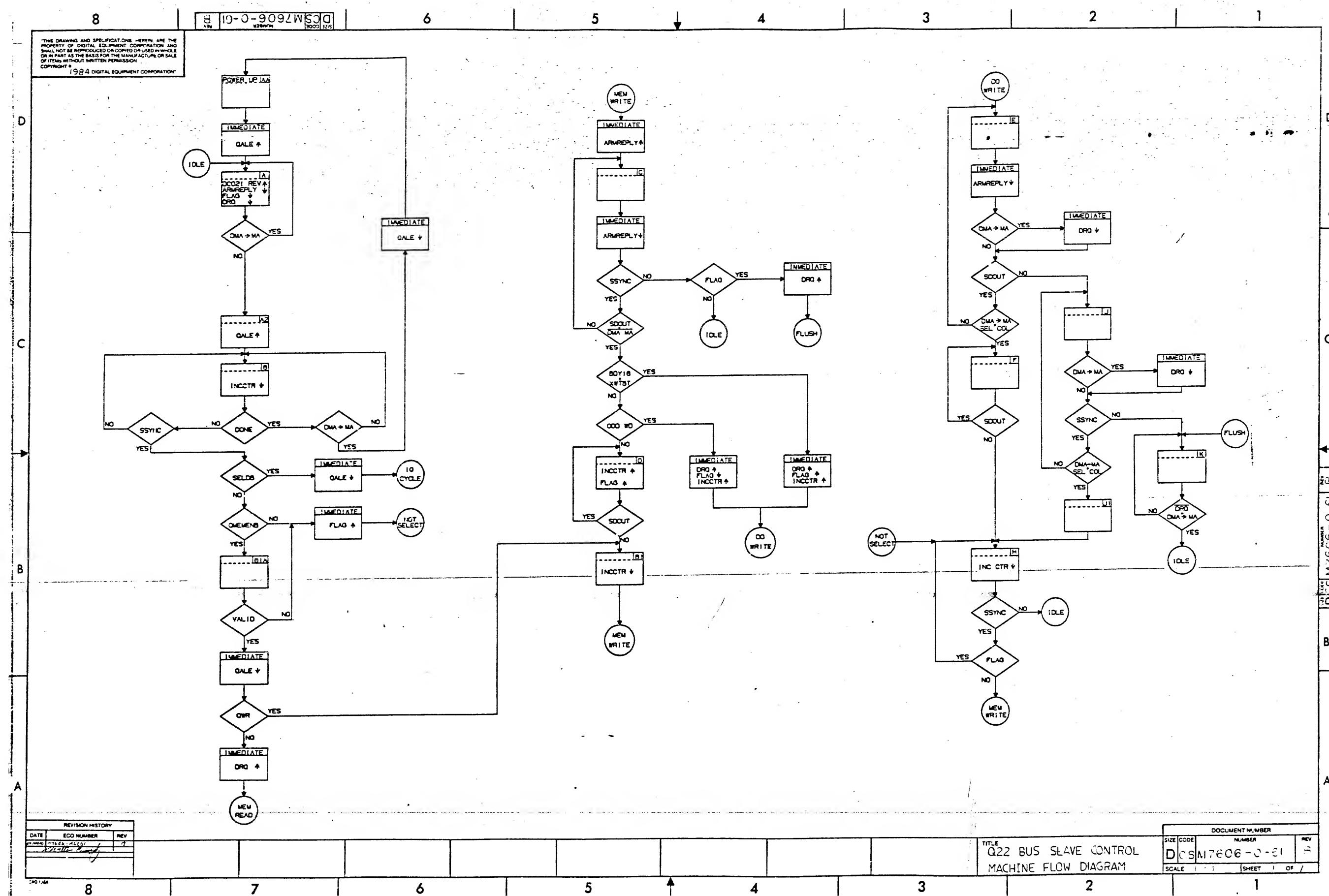
C
V
B
A

```

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REVISIONS
CHK CHANGE NO. REV

DRW. *J. Tonky* DATE 09-AUG-85 ENG. R. McNAMARA DATE 09-AUG-85 TITLE: Q22 BUS SLAVE CTL
CHK'D R. McNAMARA DATE 09-AUG-85 BOARD LOCATION:
R. McNAMARA DATE 09-AUG-85 SHEET 1 OF 1 MACHINE LISTING
DSK#7.T2P(4,550) 09-AUG-85 07:39 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: SIZE CODE NUMBER REV.
D CS M7606-0-60 A



8

B 22-0-2 DCS M17606-2

6

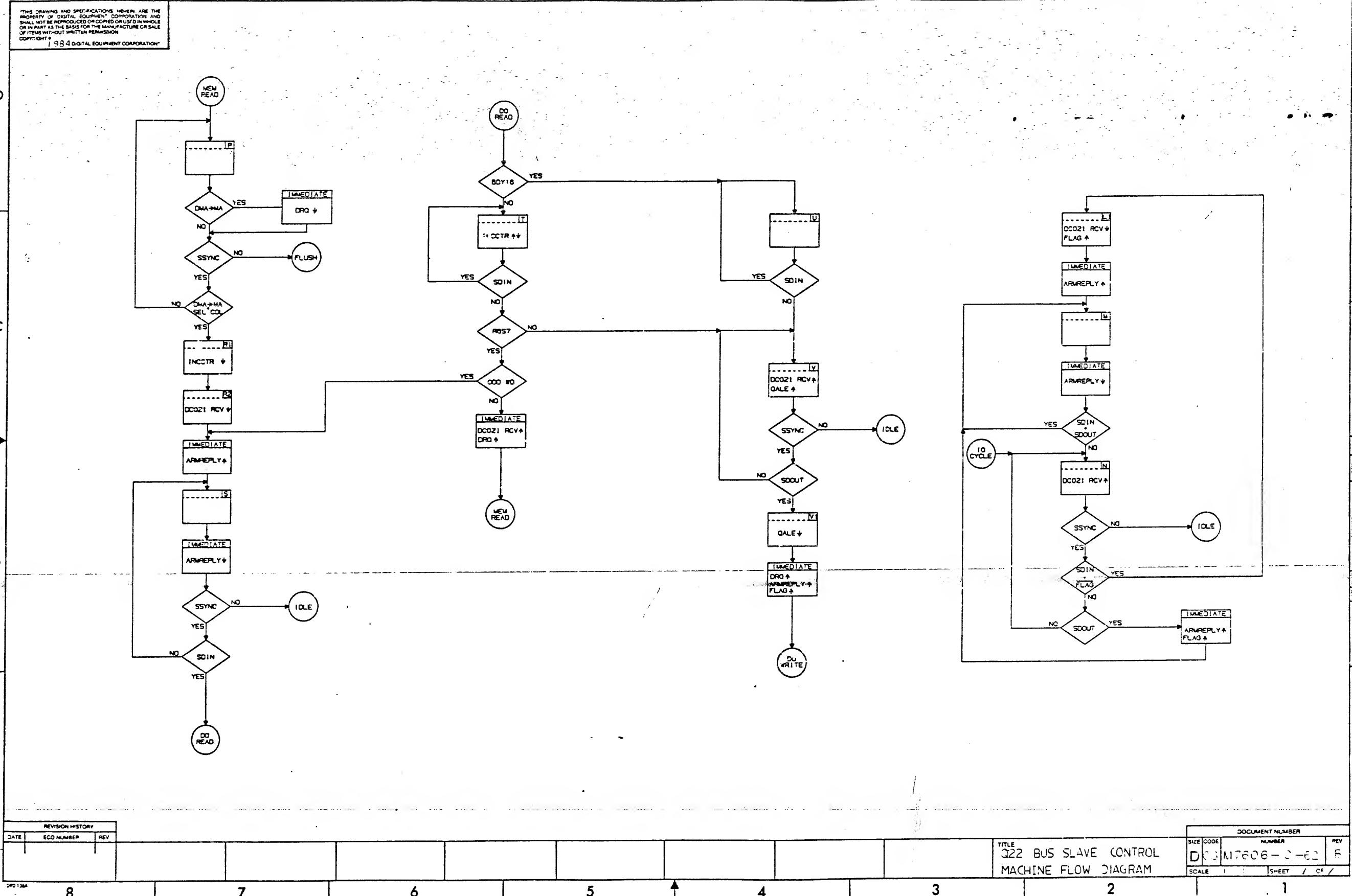
5

4

3

2

1



REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE
Q22 BUS SLAVE CONTROL
MACHINE FLOW DIAGRAM

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
D	CS	M17606-2-E2	F

SCALE 1 : 1 SHEET / CF /

DEC PART NUMBER: 23-E42F1-00 KA630 -A, -B 1MB RAS DECODE PROM < E79
DATE ORIGINATED: 10-September-1984

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040	5	077	09I	9	08R	9	0CE	9	171	9	208	9	1D3	9	219	9	297	9	2B3	9	359	9	396	9	39N	9	3D6	9			
041	5	078	09J	9	08S	9	0CE	9	172	9	209	9	1D4	9	220	9	298	9	2B4	9	360	9	397	9	39O	9	3D7	9			
042	5	079	09K	9	08T	9	0CE	9	173	9	210	9	1D5	9	221	9	299	9	2B5	9	361	9	398	9	39P	9	3D8	9			
043	5	080	09L	9	08U	9	0CE	9	174	9	211	9	1D6	9	222	9	290	9	2B6	9	362	9	399	9	39R	9	3D9	9			
044	5	081	09M	9	08V	9	0CE	9	175	9	212	9	1D7	9	223	9	291	9	2B7	9	363	9	39A	9	39S	9	3D0	9			
045	5	082	09N	9	08W	9	0CE	9	176	9	213	9	1D8	9	224	9	292	9	2B8	9	364	9	39B	9	39T	9	3D1	9			
046	5	083	09O	9	08X	9	0CE	9	177	9	214	9	1D9	9	225	9	293	9	2B9	9	365	9	39C	9	39U	9	3D2	9			
047	5	084	09P	9	08Y	9	0CE	9	178	9	215	9	1DA	9	226	9	294	9	2B0	9	366	9	39D	9	39V	9	3D3	9			
048	5	085	09Q	9	08Z	9	0CE	9	179	9	216	9	1DB	9	227	9	295	9	2B1	9	367	9	39E	9	39W	9	3D4	9			

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RE
CHK CHK

DIGITAL	DRW: <i>J. Lomby</i>	DATE: 09-AUG-85	ENG: R. MCNAMARA	DATE: 09-AUG-85	TITLE: 1KX4 RAS DECODE PROM (E79) LISTING
CHK'D:	R. MCNAMARA	DATE: 09-AUG-85	BOARD LOCATION: SHEET OF 9		
DSK#4.T2PC4.550J	09-AUG-85	07:39	NEXT HIGHER ASSEMBLY:	SIZE D	CODE CS NUMBER M7605-0-63
FIRST USED ON OPTION/MODEL:				REV. A	

8	7	6	5	V	4	3	2	D	C	B	A	1																																																																
D												D																																																																
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B												B																																																																
A												A																																																																
<p>T: PAL16L8A P: 23-169J5-00 E40 N: BARRY MASKAS D: 25 OCT 1984 S: /RPOK /BTRYOK CSMAPEMEAR /EPAS EPDS UVWR /DONE QALE /GRANT GND SRPLY /CLRPSH /ENBL5646 /WRMAP /ENBBAL RDIN DC021RCV /TDIO /RCVBDAHL VCC B: IF [VCC] CLRPSH = RPOK + BTRYOK IF [VCC] ENBL5646 = CSMAPEMEAR * EPAS IF [VCC] WRMAP = CSMAPEMEAR * UVWR * EPDS IF [VCC] ENBBAL = /GRANT * /RDIN * /DONE + GRANT * /DONE * QALE + /DC021RCV * /GRANT * /DONE IF [VCC] RCVBDAHL = /TDIO * /DC021RCV + /TDIO * GRANT + /SRPLY * /DC021RCV + /SRPLY * GRANT + UVWR * /DC021RCV + UVWR * GRANT E: KA630-A, -B, -C, -D (M7606) MISC. CONTROL STROBES</p> <p>T: PAL16L8A P: 23-170J5-00 E78 N: BARRY MASKAS D: 25 OCT 1984 S: /PE3 /PE2 /PE1 /PE0 /MSERO /MEMWR /BYTACT3 /BYTACT2 /BYTACT1 GND /BYTACT0 /HI16PER /LO16PER /PERR /SELCOL /ENBCAS0H /ENBCAS1H /ENBCAS2H /ENBCAS3H VCC B: IF [VCC] HI16PER = MSERO * PE2 * BYTACT2 + MSERO * PE3 * BYTACT3 IF [VCC] LO16PER = MSERO * PE0 * BYTACT0 + MSERO * PE1 * BYTACT1 IF [VCC] PERR = MSERO * MEMWR * PE0 * BYTACT0 + MSERO * MEMWR * PE1 * BYTACT1 + MSERO * MEMWR * PE2 * BYTACT2 + MSERO * MEMWR * PE3 * BYTACT3 IF [VCC] ENBCAS0H = /SELCOL + /BYTACT0 IF [VCC] ENBCAS1H = /SELCOL + /BYTACT1 IF [VCC] ENBCAS2H = /SELCOL + /BYTACT2 IF [VCC] ENBCAS3H = /SELCOL + /BYTACT3 E: KA630-A, -B, -C, -D (M7606) MEMORY SYSTEM CAS CONTROL STROBES AND PARITY ERROR DETECTION STROBES</p> <p>T: PAL16L8A P: 23-171J5-00 E86 N: BARRY MASKAS D: 25 OCT 1984 S: /UVCYCCD2 /DMAMA /DONE /MSER1 /UVCYC /MEMWR DECODE /DATABUFENB MEMCD0 GND MEMCD1 /MSWTOH /MSWT1H SELCOL /BUFENB /BUFENB0 /BUFENB1 /BDIRT /STARTCYC VCC B: IF [VCC] MSWTOH = /MEMCD1 + MEMCD0 + /MEMWR + /UVCYC IF [VCC] MSWT1H = MEMCD1 + /MEMWR + /UVCYC IF [VCC] BUFENB = MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + MEMCD1 * /MEMCD0 * MEMWR * UVCYC * MSER1 IF [VCC] BUFENB0 = /MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + /MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 * MEMCD0 * MEMWR * UVCYC * MSER1 IF [VCC] BUFENB1 = /MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + /MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 * /MEMCD0 * /MEMWR * UVCYC * MSER1 IF [VCC] BDIRT = MEMWR * DECODE + MEMWR * SELCOL * MSER1 IF [VCC] STARTCYC = /DMAMA * UVCYCCD2 * UVCYC * /MEMWR + /DMAMA * DECODE * /UVCYCCD2 * UVCYC * /MEMWR * DONE + /DMAMA * UVCYC * MEMWR * DMAMA * DECODE + DMAMA * SELCOL E: KA630-A, -B, -C, -D (M7606) MEMORY SUBSYSTEM BUFFER CONTROL STROBES AND MEMORY CYCLE ENABLE STROBE</p>																																																																												
<p>THIS DRAWING AND SPECIFICATIONS HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION. DUALLY NOT REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHIN WRITTEN PERMISSION. © 1984, DIGITAL EQUIPMENT CORPORATION.</p> <table border="1"> <tr> <td>REVISIONS</td><td>CHK CHANGE NO.</td><td>REV.</td> <td>digital</td><td>DRW. <i>S. Jourby</i></td><td>DATE 09-AUG-85</td><td>ENG. R. McNAMARA</td><td>DATE 09-AUG-85</td><td colspan="5">TITLE: PALASM LISTINGS FOR PAL16L8A DEVICES</td> </tr> <tr> <td></td><td></td><td></td><td></td><td>CHK'D</td><td></td><td>BOARD LOCATION:</td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td></td><td></td><td></td><td></td><td>R. McNAMARA</td><td>09-AUG-85</td><td>SHEET 1 OF 1</td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td></td><td></td><td></td><td></td><td>DSK:3.12P(4,550)</td><td>109-AUG-85 07:39</td><td>NEXT HIGHER ASSEMBLY:</td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td></td><td></td><td></td><td></td><td colspan="5">FIRST USED ON OPTION/MODEL:</td><td>SIZE CODE D</td><td>NUMBER M7606-0-64</td><td>REV. A</td><td></td> </tr> </table>	REVISIONS	CHK CHANGE NO.	REV.	digital	DRW. <i>S. Jourby</i>	DATE 09-AUG-85	ENG. R. McNAMARA	DATE 09-AUG-85	TITLE: PALASM LISTINGS FOR PAL16L8A DEVICES									CHK'D		BOARD LOCATION:											R. McNAMARA	09-AUG-85	SHEET 1 OF 1											DSK:3.12P(4,550)	109-AUG-85 07:39	NEXT HIGHER ASSEMBLY:											FIRST USED ON OPTION/MODEL:					SIZE CODE D	NUMBER M7606-0-64	REV. A												
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+12.0V raw +12 volts
+3VA logic "high" voltage
+5.0V raw +5 volts
-12.0V charge pump generated -12 volts
ARB(L) asserted if module is bus arbiter
ARM REPLY(L) sets ENBREPLY (inside Qbus gate array)
ARM UDALK(L) asserted to enable the uVDAL <-> MD transceivers
ARMRDYERR(L) indicates that memory arbiter is READY to finish a cycle
ASYNC T.O.(H) Q-bus timeout
AUX HALT(H) auxiliary processor halt
BBS7(L) Qbus BS7 (selects I/O page, used in block mode handshake)
BDAL<21:0>L Qbus data/address lines
BDCOK(H) Qbus DCOK signal (indicates DC power at proper level)
BDG CD<1:0>L firmware mode select from configuration connector to BDR
BDIN(L) Qbus DIN control signal
BDIR(L) dram buffer direction transmit enable
BDMG(L) Qbus DMGI (DMA grant in)
BDMGO(L) Qbus DMGO (DMA grant out)
BCMRL(L) Qbus DMR (DMA request)
BDOUT(L) Qbus DOUT control signal
BDR<3:0>L boot and diagnostic register LED controls
BDY16(L) indicates address is at a 16 word boundary
BEVENT(L) Qbus EVENT signal (terminated but not used)
BHALT(L) Qbus HALT signal
BIAK(L) Qbus IAKI (interrupt acknowledge in)
BIAKO(L) Qbus IAKO (interrupt acknowledge out)
BINIT(L) Qbus INIT signal (clobbers/init everybody on bus)
BIRQ<7:4>L Qbus IRQ lines (interrupt requests)
BMAA<8:0>H buffered and damped local dram array address signals
BMCAS<3:0>H byte active controlled unbuffered column address strobes
BMSWT<0>L buffered and damped local dram array write signal
BP0K(H) Qbus POK signal (indicates sufficient power for operation)
BREAK(H) serial line break indication from DLART
BREF(L) Qbus REF signal (used in block mode handshake)
BRPLY(L) Qbus RPLY control signal (reply)
BRS<2:0>L bit rate selection (from back panel into DLART)
BSACK(L) Qbus SACK control signal (bus acknowledgement)
BSYNC(L) Qbus SYNC control signal (strobes address, frames transactions)
BTRY OK(L) indicates battery voltage above minimum threshold
BTTRYV(H) raw battery voltage from back panel
BTVREF(H) battery or system voltage supply to watch/ram (TOY) chip
BUF ENB(L) battery supplied reference voltage (used to detect the battery)
BUF ENB<1:0>L local dram array data transceiver receive direction enable
BUVAS(H) expansion dram array data transceiver receive direction enable
BUVAS(L) buffered uvax address strobe
BUVASK(L) buffered uvax address strobe
BUVCLK0(H) buffered uvax clock out
BUVRESET(H) buffered uvax reset
BUVRESET(L) buffered uvax reset
BTBT(L) Qbus WTBT signal (indicates write cycle, and byte write)
BYTACT<3:0>L byte active bits to mem sequencer
CAS<3:0>L buffered and damped local dram array column address strobes
CLK 614.4KHZ(H) clock from 614.4KHz oscillator
CLK 614.4KHZ(L) clock from 614.4KHz oscillator
CLK031(H) clock from 32KHz oscillator (31us period)
CLK25(H) clock from 40MHz oscillator (25ns period)
CLR PS(H) clear power sense in TOY clock
CONF<3:2>L configuration connector buffered inputs (see table on 1.10)
CS DL(L) chip select for DLART
CS MAP(L) chip select for MAP

CS MAP;EMEAR(H) chip select for MAP or EMEAR (external mem. err. addr. reg.)
CS PROM(L) chip select for PROM
CS TOY(H) chip select for TOY
CTL_XDAL<1:0>H address function bits (see table on 1.7)
DATA BUF ENBKL abus slave memory cycle
DC021RCV(H) controls direction of DC021 during slave mode transactions
DECODE(H) allows memory sequencer to decode and RAS memory
DLADK<1:0>H the two lo-order address lines for the DLART
DLRD(L) read signal for DLART
DLRRQ(H) receiver interrupt from DLART
DL_SIK(H) serial data in (to DLART)
DLSOC(H) serial data out (from DLART)
DLWR(L) write signal for DLART
DLXRQ(H) transmitter interrupt from DLART
DMA->MA(L) "DMA acknowledge" from main memory state machine
DOK(H) delayed indication of DC power at proper level
DONE(L) indicates that requested transaction is completed
DRDCOK(H) delayed indication of DC power at proper level
DRQ(L) DMA request to main memory state machine
ENB 8641(L) enable for Qbus drivers (for disabling drivers at power up)
ENB BDAL(L) output enable for DC021 xcurs
ENB CAS<3:0>H select column and byte active controlled
ENB DAL(L) column address strobe enables
ENB DATA(L) enable data/address onto Q-bus
ENB LS646(L) mix'd output; enables data onto Q-bus (write),
EPAD ENB(L) or strobes data in from Q-bus (read)
EPAC<1>H output enable control strobe for EPR <-> XLAT AD transceivers
EPAS(L) external processor bus (local I/O bus) address enable
EPDSCH external processor bus (local I/O bus) address control
EPDK<15:0>H delayed indication of DC power at proper level
EPREADY(L) external processor bus (local I/O bus) data strobe
FORCEINIT(H) auxiliary machine arm for DC379 READY or uVERR logic
FSTRDY(H) assertion forces arbitration machine to reset and assert TINIT
GRANT(L) low 16 mega-byte normal (fast) uvax ready strobe
HI16PER(L) Q-bus grant sent to Q-bus Master state machine
HIROMDLATCH(L) high word parity error from memory sequencer
HLT ENB(L) signals uvax intfce gate array to latch hi-order rom data
INC CTR(H) configuration connector buffered halt enable mask and BDR flag
INITRQ(L) increments block mode address counter
INTRVL TIM(L) init request from uvax's bus init register
IRQ<7:5>L interval timer 10ms
LO16MB(L) uvax interrupt request inputs for processor levels 17, 16, 15
LC16PER(L) indicates address is in low 16 MB of 30 bit address space
LOCAL NXMH(Y) low word parity error from memory sequencer
LOCK(L) low 16 mega-byte non-existent physical memory flag
LOCK(L) asserted if uvax is doing "read lock/write unlock"
LPDK<3:0>H local dram array transceiver generated byte parity data bits
LRD<31:0>H local dram array transceiver data bits
LPERR(L) local low 16 mega-byte dram parity error strobe
MA<23:2>H memory address bus
MAA<9:0>L row/column multiplexed memory address bus
MAP AD<21:9>H RDAL bits 21:9 latched for translation map
MAP DISABLE(H) scatter/gather map ram output enable control
MBMARB<8:0>H local dram array buffered address signals
MBMSWT<0>L local dram array buffered write strobe
MCAS<3:0>L local dram array buffered column address strobes
MDK 31:0>H 32 bit memory data bus
MEM CD<1:0>H memory array selection codes (see 2.1.2)
MEMWR(L) indicates a write to memory

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

REV. A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

SIZE CODE CS M7606-0-65

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REVISIONS CHK CHANGE NO. REV

digital	DRA. 1000	DATE 09-AUG-85	ENG. R. McNAMARA	DATE 09-AUG-85	TITLE: MNEMONIC DICTIONARY
CHK'D	DATE 09-AUG-85	BOARD LOCATION: SHEET 1 OF 2	R. McNAMARA	DATE 09-AUG-85	
DSK#1.T2PC4,550	09-AUG-85 02:38	NEXT HIGHER ASSEMBLY:			
FIRST USED ON OPTION/MODEL:					SIZE CODE NUMBER REV.

8 7 6 5 4 3 2 1

D
 MRAS<81:80>L local dram array buffered row address strobes
 MSER<1:0>L memory system error register write wrong parity and parity trap enable controls
 MSID<4:0>L expansion memory identification codes
 MSWT<1:0>H expansion memory write control strobes
 ODD WD<H> indicates an odd word address
 OSC031<H> watch/ram (TOY chip) clock input (31us)
 PD<3:2>H local dram array parity data
 LPD<3:0>H local dram array damped parity data
 PE<3:0>L dram array transceiver (wire-ored) byte parity error strobes
 PERR<L> local dram array byte active and select column controlled parity error strobe
 PF(L) power failure strobe
 QALE(H) Q-bus address latch enable (also indicates "slave idle")
 QBIQCYC(L) uVAX is addressing Q-bus I/O space (not memory)
 QMENB(L) enables Q-bus access to local memory
 QRQ(L) Q-bus request from uVAX
 QWR(H) WTBT input from Q-bus (latched at assertion of SYNC)
 RAS ALL<H> generates RAS for all memory banks during refresh
 RAS DECODE<L> row address strobe decoder enable
 RAS<81:80>L buffered and damped local dram array raw address strobes
 RAS<8:0>H nine row address strobes for the nine possible banks of dram
 RBS7<H> BS7 input from Q-bus
 RCV BDAL<P> controls the direction of the DC021 xcvr's
 RD<31:16>h undamped local dram array data transceiver data lines
 RDCOK<L> indicates DC power at proper level
 RDIN<H> DIN from the Q-bus
 RDG1<H> DMGI from the Q-bus
 RDMR<H> DMR from the Q-bus
 RDOUT<H> DOUT from the Q-bus
 READY<H> DC379 generated uVAX ready strobe, armed by EREADY
 REF REQ<H> indicates a refresh cycle needed
 REF->MA(L) clears a refresh request & enables ref adrs onto MA
 RHALT<H> HALT from the Q-bus
 RIAKI<H> IAKI from the Q-bus
 RINIT<H> INIT from the Q-bus
 RIRQ<7:4>H IRQ's from the Q-bus
 RPOK<L> POK from the Q-bus
 RR<H> sync'd refresh request (to memory arbiter)
 RREF<H> REF from the Q-bus
 RRPLY<H> RPLY from the Q-bus
 RSACK<H> SACK from the Q-bus
 RSYNC<H> SYNC input from Q-bus
 RSYNC<L> inverted SYNC for latching XDAL's for scatter/gather map
 RUNK<L> exited halt protected prom and prefetching and dram refreshing status flag
 SDIN<H> sync'd DIN from the Q-bus
 SDMG1<H> sync'd DMGI from the Q-bus
 SDMR<H> sync'd DMR from the Q-bus
 SDOUT<H> sync'd DOUT from the Q-bus
 SEL DBCL<L> Q-bus doorbell select
 SEL L016MB<L> dynamic low 16 mega-byte address comparitor output
 SELCOL<H> RAM timing signal (indicates existing memory)
 SELCOL<L> RAM timing signal (indicates existing memory)
 SG1<L> soft ground (for use by board testers)
 SG4<L> soft ground (for use by board testers)
 SI<H> terminated eia serial in +
 SI<L> terminated eia serial in -
 SRPLY<H> sync'd RPLY input from Q-bus
 SRUNK<L> goes to "RUN" light on front panel

SSACK<H> sync'd SACK input from Q-bus
 SSYNC<H> sync'd SYNC input from Q-bus
 START CYC<L> select column control for lock or non-existent memory cycles
 SYSCLK<H> unbuffered system clock used to drive uVAX and FPU
 T.O.<H> sync'd 10 usec. timeout
 TBSZ<H> BS7 output to Q-bus
 TDIO<L> TDIN or TDOUT control from Q-bus master state machine
 TDMG0<H> DMGO output to Q-bus
 TDMR<H> DMR output to Q-bus
 TIAKO<H> IAKO output to Q-bus
 TINIT<H> INIT output to Q-bus (externally gated by ARB)
 TREFC<H> REF output to Q-bus
 TRPLY<H> TRPLY output to Q-bus
 TSK1<H> "t-state" counter outputs (sync'd to uVAX ucycle at power up)
 TSK1<L> "t-state" grey code counter Inverted feedback next state control
 TSACK<H> SACK output to Q-bus
 TSYNC<H> SYNC output to Q-bus
 UVAS<L> uVAX address strobe
 UVBR<3:0>L byte mask bits from uvax
 UVBR<14>L bus interrupt request input for processor level 14
 UVCLK0<H> unbuffered uVAX clock out
 UVC5<2:0>H uVAX cycle status strobes (see table on 1.1)
 UVCY<L> low 16 mega-byte dram cycle started flag
 (enables select column strobe)
 UVCYCCD<2:0>L uVAX cycle codes (see table on 1.7)
 UVDAL->MA(L) enables uVAX latched addresses onto MA bus
 UVDAL<31:0>H uVAX data/address lines
 UVDBE<L> uVAX data buffer enable strobe
 UVDS<L> uVAX data strobe
 UVEPS<L> uVAX external processor strobe
 UVERR<L> uVAX error (forces abnormal termination of cycle)
 UVHALT<L> uVAX halt
 UVRDY<L> uVAX ready control input
 UVRESET<L> uVAX reset control signal
 UVWR<H> buffered uVAX write signal
 UVWR<L> uVAX write signal
 V1.2REF<H> 1.2 volt reference in battery sense circuit
 V4.3REF<H> 4.3 volt regulator in charge pump circuit
 VALID<H> valid bit from "scatter-gather" map
 WR MAP<L> write control signal for map
 XDAL<21:0>H address/data in-out from Q-bus
 XDB1 RQ<H> doorbell interrupt request
 XDMA QPE<H> Q-bus parity error on a Q-bus read cycle
 XLAT AD<23:9>H translated addresses out of scatter/gather map
 XWTBT<H> WTBT input from Q-bus

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REVISIONS
 CHK CHANGE NO. REV

DATE: 09-AUG-85 ENG: R. McNAMARA DATE: 09-AUG-85 TITLE: MNEMONIC
 CHK'D R. McNAMARA DATE: 09-AUG-85 BOARD LOCATION:
 DSK:2.T2PC4,5501 09-AUG-85 07:38 SHEET: 2 OF 2
 FIRST USED ON OPTION/MODEL: SIZE CODE NUMBER REV.
 D CS M7606-0-65 A

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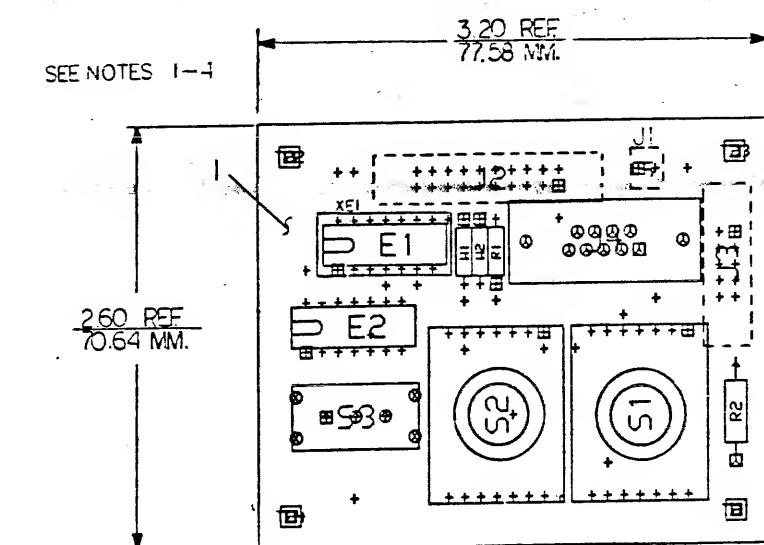
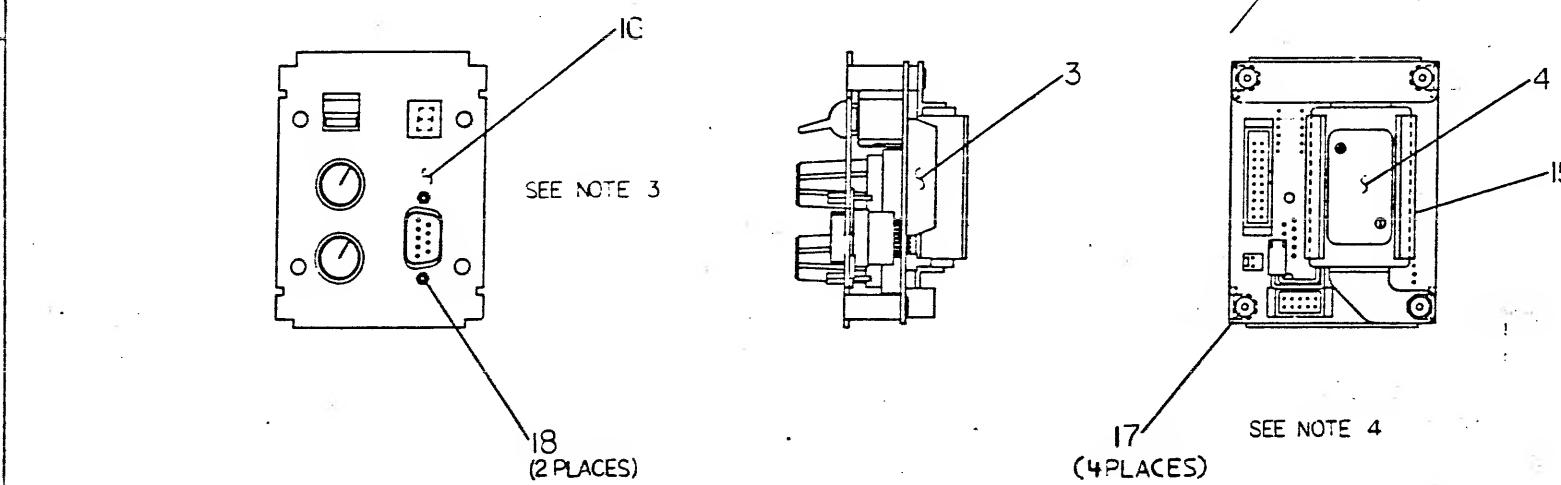
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NOTES:

- W1 W2 ARE NOT INSTALLED.
- 2, 12 AND 13 ARE MOUNTED ON SIDE 2.
- 3. MOUNT J4 TO ITEM 16 WITH ITEM 19 BEFORE SOLDERING INTO ITEM 1.
- 4. TEST PANEL IN TESTER AFTER COMPLETING NOTE 3 AND BEFORE ASSEMBLY OF ITEMS 115, 16 WITH ITEM 17.
- STEP E → Y AXIS STEP TIMES
- REPEAT → X AXIS STEP TIMES

CHG	CHANGE NO	REV	SIGNATURE	DATE
2	SIGNATURE	B	DAVID DROZD	1985
3	SIGNATURE	B	CHK D.	1985
4	SIGNATURE	B	MECH. ENG.	1985

ETCH REV.	A1
3	
2	

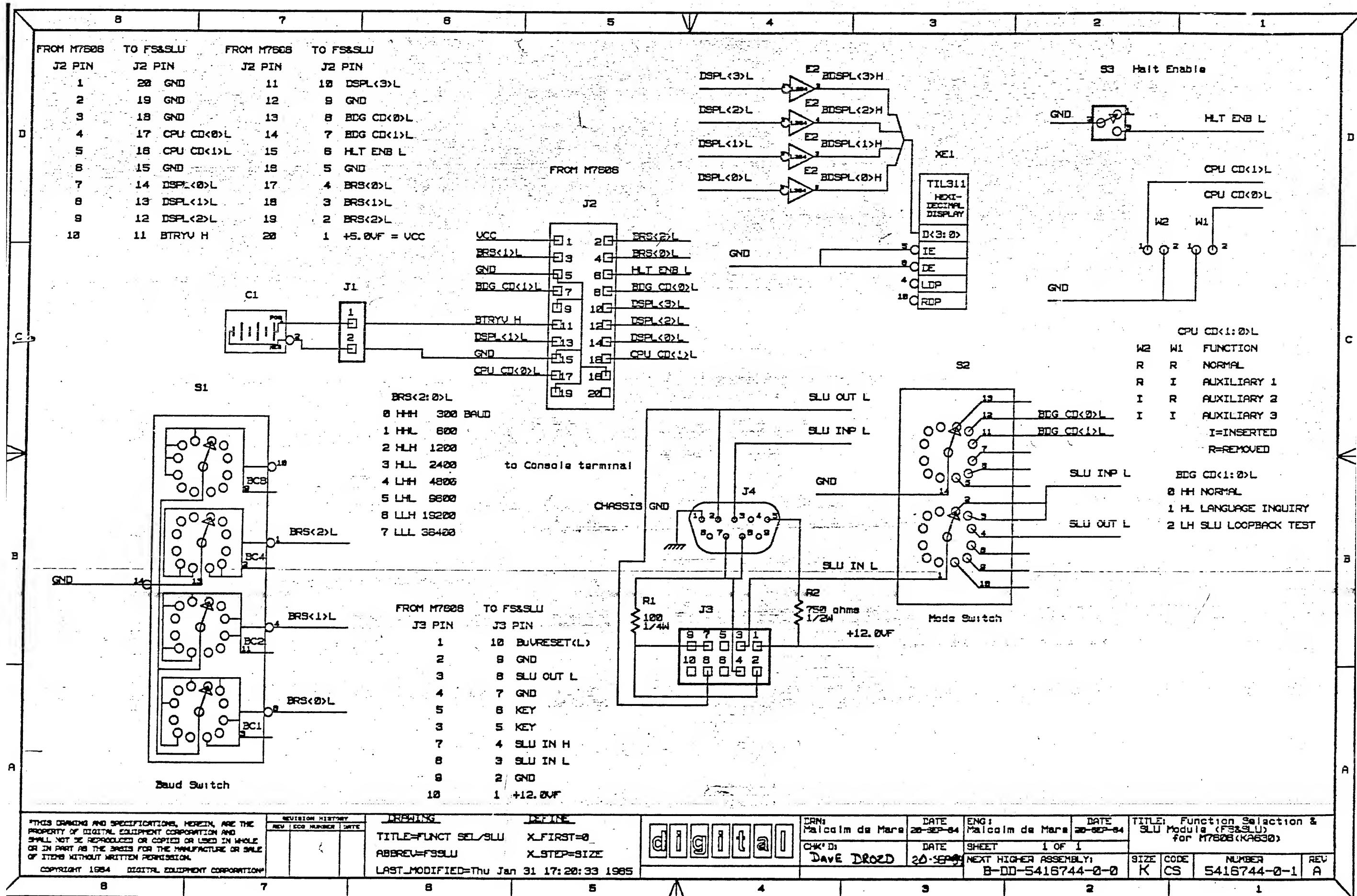
SIGNATURES	DATE	digital
DRN. DAVID DROZD	1985	
CHK D.	1985	
MECH. ENG.	1985	TITLE FUNCTION
PROJ. ENG. 14 de Mar	1985	SEL / SLU
PROD. 14 de Mar	1985	
SCALE 2/1	SIZE CODE	NUMBER
SHT. 1 OF	D UA	54167-4-0-0
NEXT HIGHER ASSY. B-DD-5416744-0-0		

1 MS # 275100

LINE ITEM	TOP DOCUMENT	PART NUMBER	REV	DESCRIPTION	MIN	VARIATION REVISION LEVEL:	QTY PER VARIATION	REFERENCE DESIGNATOR
1	1	D-MD-5016743-0-0	5016743-01	CIRCUIT DRILL AND ETCH		1		
2	2		1216565-02	SKT, IC 14PIN DIP TIN ELEV		1		XE1
3	3		1217727-00	PCB, HEADER 20POS(1X20).100CC STR		1		J2
4	4		1219245-01	BATTERY, 3CELL 3.75V .18MA NICAD		1		
5	5		1219251-00	PCB HEADER 02PIN(1X02).100CC STR		1		J1
6	6		1219573-05	CONN, D SUB 9PIN ASSY STR		1		J4
7	7		1219952-08	PCB HEADER 09PIN(2X05).100CC STR		1		J3
8	8		1223262-01	SW,ROT 1P08POS		1		S1
9	9		1223263-02	SW,ROT 2P03POS		1		S2
10	10		1223646-01	SW,RKR SPDT ON-OFF-ON		1		S3
11	11		1300229-00	100.0 .25 W 5.0 % CF		1		R1
12	12		1300354-00	750.0 .50 W 5.0 % CF		1		R2
13	13		1912803-00	LS04 INVERTER GATE,HEX		1		E2
14	14		1916921-00	HEXADECIMAL DISPLAY W/DECODER		1		E1
15	15		7430801-01	HOLDER,BATTERY		1		
16	16		7431737-01	PLATE,CONNECTOR		1		
17	17		9008181-01	SCREW,TAP PAN PHIL 6-		4		
18	18		9008451-01	SCREW LOCK,STANDOFF ONLY .060TH		2		

REVISION HISTORY			BASIC PART NO: 5416744		DRN:	E. LANDRY	DATE: 01-JUN-84	D I G I T A L
ENG	ECO NUMBER	REV	SECTION A OF A		CHK'D:	D. DROZD	DATE: 01-JUN-84	TITLE PARTS LIST FUNCTION SEL/SLU MODULE
INITIAL			A	SECTION VARIATION INDEX	DES.ENG:	M. DEMARE	DATE: 12-OCT-84	DOCUMENT NUMBER
				[A] 01				SIZE!CODE! NUMBER REV
				[B]				
				[C]				
				[D]				
				[E]				
				[F]				
				[G]				
				[H]				
				[I]				
				[J]				
				[K]				
				[L]				
				[M]				
				[N]				
					ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:	EDIT #
					D-UA-5416744-0-0	D-UA-5416744-0-OP	ML769A.PLS	34

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digital

DRN. BARRY CORMIER	DATE 11/9/84	TITLE GRANT CONTINUITY			
CHK'D J.CUNNINGHAM	DATE 11/9/84				
DES. ENG. R. LEAZER	DATE 11/14/84	DOCUMENT NUMBER M9047-0-0			
RESP. ENG. R. LEAZER	DATE 11/14/84				
MFG. ENG. A. BROOKS	DATE 11/14/84	SIZE B	CODE DD	NUMBER M9047-0-0	REV. B
				SHEET 1	OF 1

8	7	6	5	4	3	2	1										
				↓													
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1995																	
COMPONENT SIDE VIEW																	
<p>NOTES:</p> <p>STEP E ↑ Y AXIS STEP TIMES REPEAT → X AXIS STEP TIMES</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>CHK CHANGE NO</td> <td>REV</td> </tr> <tr> <td>ASSEMBLY 001</td> <td>B</td> </tr> <tr> <td>FILE NUMBER</td> <td>100-1000</td> </tr> <tr> <td>DATE</td> <td>10/95</td> </tr> </table>								CHK CHANGE NO	REV	ASSEMBLY 001	B	FILE NUMBER	100-1000	DATE	10/95		
CHK CHANGE NO	REV																
ASSEMBLY 001	B																
FILE NUMBER	100-1000																
DATE	10/95																
<p>SIGNATURES DATE</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>DRN. E. LANDRY</td> <td>10/2/95</td> </tr> <tr> <td>CHK D. ALLEN</td> <td>10/2/95</td> </tr> <tr> <td>MECH. ENG. [Signature]</td> <td>10/2/95</td> </tr> <tr> <td>PROJ. ENG. [Signature]</td> <td>10/2/95</td> </tr> <tr> <td>PROD. [Signature]</td> <td>10/2/95</td> </tr> </table> <p>digital</p> <p>TITLE GRANT CONTINUITY</p> <p>ETCH REV. B1-P2</p> <p>SCALE 2/1</p> <p>SHT. 1 OF 1</p> <p>SIZE CODE NUMBER REV</p> <p>D UA 19047-0-0 B</p> <p>NEXT HIGHER ASSY. B-00-19047-0-0</p>								DRN. E. LANDRY	10/2/95	CHK D. ALLEN	10/2/95	MECH. ENG. [Signature]	10/2/95	PROJ. ENG. [Signature]	10/2/95	PROD. [Signature]	10/2/95
DRN. E. LANDRY	10/2/95																
CHK D. ALLEN	10/2/95																
MECH. ENG. [Signature]	10/2/95																
PROJ. ENG. [Signature]	10/2/95																
PROD. [Signature]	10/2/95																
1 MS# 27546																	

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REVISION HISTORY	DATE	ECO NUMBER	REV
000 103			

OPEN	<i>David Day</i>	DATE	2-26-85	TITLE	<i>digital</i>
CHEKED	<i>Ed Landry</i>	DATE	2-27-85		
DATE FILED	<i>Berry/Melvin</i>	DATE	2-27-85		
REF ID#	<i>Barry/Melvin</i>	DATE	2-27-85		
TYPE	<i>Sherry Marshall</i>	DATE	2-27-85		
MOT HIGHEST DOC.				DOCUMENT NUMBER	
B-00-M9047-0 -0				FILE #	M9047-0-1 A
				SCALE	INCHES
				SHIRT	OF

LINE ITEM	TOP DOCUMENT	MIN	PART NUMBER	REV	DESCRIPTION	VARIATION	REVISION LEVEL:	QTY PER VARIATION	
								01	02
1	1	A-PS-1700313-0-0	1700313-01	A	CABLE ASSY,06 COND,MOLD,SHLD	2	1		
2	2	A-PS-4700042-0-0	4700042-01		SCREWDRIVER,FLAT BLADE 0.12 X 2.		1	1	
3	3	A-PS-3622092-0-0	3622092-01	A	LABEL,LCP5 CONFIGURATION		1	1	
4	4	A-PS-9907349-0-0	9907349-01	A	CARTON,DIECUT,C,200PSI,W/GRAPHIC		1	1	
5	5	B-DD-M9047-0	M9047-00		QBUS GRANT CONTINUITY,1ST USED I		1	1	
6	6	A-PS-1700301-0-0	1700301-00	A	CABLE ASSY,07 COND,MOLD,SHLD	2	1		
7	7	A-PS-3624251-0-0	3624251-01	A	LABEL,FRONT CONTROL PANEL BA123		1	1	

REVISION HISTORY			BASIC PART NO: 7022382	DRN:	D. HEALY	DATE: 05-DEC-84	D	I	G	I	T	A	L
ENG	ECO NUMBER	REV	SECTION A OF A	CHK'D:	D. HEALY	DATE: 08-MAR-85	TITLE PARTS LIST						
	INITIAL	A	SECTION.VARIATION INDEX [A]01,02	DES.ENG:	J. KWONG	DATE: 08-MAR-85	BA123-A ACCESSORY KIT						
			[B]	RESP.ENG.:	J. KWONG	DATE: 08-MAR-85	DOCUMENT NUMBER						
			[C]	MFG.ENG.:	J. EDWARDS	DATE: 08-MAR-85	SIZE	CODE	NUMBER	REV			
			[D]	ASSEMBLY NUMBER:		DATE: 08-MAR-85	K	PL	7022382-0-DBP	A			
			[E]	TOP DOCUMENT NUMBER:		RELEASE DATE: 26-MAR-85							
			[F]	FILE NAME:		EDIT #							
				ML755A.PLS		4							

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FIELD MAINTENANCE PRINT SET

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TABLE OF CONTENTS

B - TC - 7022380 - 0 - DBU	BA123-A BASIC ENCLOSURE (TC)
D - AD - 7022380 - 0 - DBU	BA123-A BASIC ENCLOSURE
K - PL - 7022380 - 0 - DBP	BA123-A BASIC ENCLOSURE (PL)
B - DD - 7022380 - 0 - DBU	BA123-A BASIC ENCLOSURE (DD ONLY)
D - AR - 7022380 - 0 - DBU	BA123-A SYSTEM ARRANGEMENT
B - DD - 5417507 - 0 - 0	QBUS BACKPLANE 13 SLOTS QUAD (DD)
K - PL - 5417507 - 0 - DBP	QBUS BACKPLANE 13 SLOTS QUAD
D - UA - 5417507 - 0 - 0	QBUS BACKPLANE 13 SLOTS QUAD
D - CS - 5417507 - 0 - 1	QBUS BACKPLANE 13 SLOTS QUAD
B - DD - 5416596 - 0 - 0	BA123-A FRONT PANEL (DD ONLY)
K - PL - 5416596 - 0 - DBP	BA123-A FRONT PANEL
D - UA - 5416596 - 0 - DBU	BA123-A FRONT PANEL
D - CS - 5416596 - 0 - 1	BA123-A FRONT PANEL
B - DD - 5416665 - 0 - 0	REMOTE SENSE TEMP (DD ONLY)
K - PL - 5416665 - 0 - DBP	REMOTE SENSE TEMP
D - UA - 5416665 - 0 - 0	REMOTE SENSE TEMP
D - CS - 5416665 - 0 - 1	REMOTE SENSE TEMP
A - PS - 1700859 - 0 - 0	CABLE, ASSY AC ON/OFF PWR
A - PS - 1700865 - 0 - 0	CABLE, 18 COND P.S. TO BACK PNL
A - PS - 1700942 - 0 - 0	CABLE ASSY, FAN DOOR INTERLOCK
A - PS - 1700863 - 0 - 0	CABLE, P.S. TO CC FAN & SENSOR
A - PS - 1700860 - 0 - 0	CABLE, ASSY, CONSOLE BACKPLANE
A - PS - 1700870 - 0 - 0	CABLE, PS TO 2 DRIVES
A - PS - 1700911 - 0 - 0	CABLE, PS TO 3 DRIVES
A - PS - 1700083 - 0 - 0	US LINE CORD
A - PS - 3023616 - 0 - 0	P.S. 460W (H7260)

**UNIT VARIATIONS
COVERED BY THIS
PRINT SET**

7022380-A2

7022380
FIELD MAINTENANCE
PRINT SET

DIGITAL EQUIPMENT
CORPORATION

PRINT SET PART
NUMBER MP-02049-01
REV A1

FILE NAME: TC7022380-0-DBUA

REVISION HISTORY		INITIAL	ECO NUMBER	REV.	BA123-A BASIC ENCLOSURE			
DATE	REV.				DRN.	DATE	TITLE	SIZE
	A	D. HEALY	29 NOV 84				digital	
	/	CHK'D D. HEALY	08 MAR 85					
		DES. ENG. J. KWONG	08 MAR 85					
		RESP. ENG. J. KWONG	08 MAR 85					
		FIELD SERVICE J. EVANS	08 MAR 85					
		TOP DOC.						
		A-DO-7022380-0-DBU						
							SHEET 1 OF 1	

MLO 1

8	7	6	5	4	3	2	1
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LEGEND
 PART NO. REV. VARIATION
 7022380-01 A1 120V
 7022380-02 A1 240V

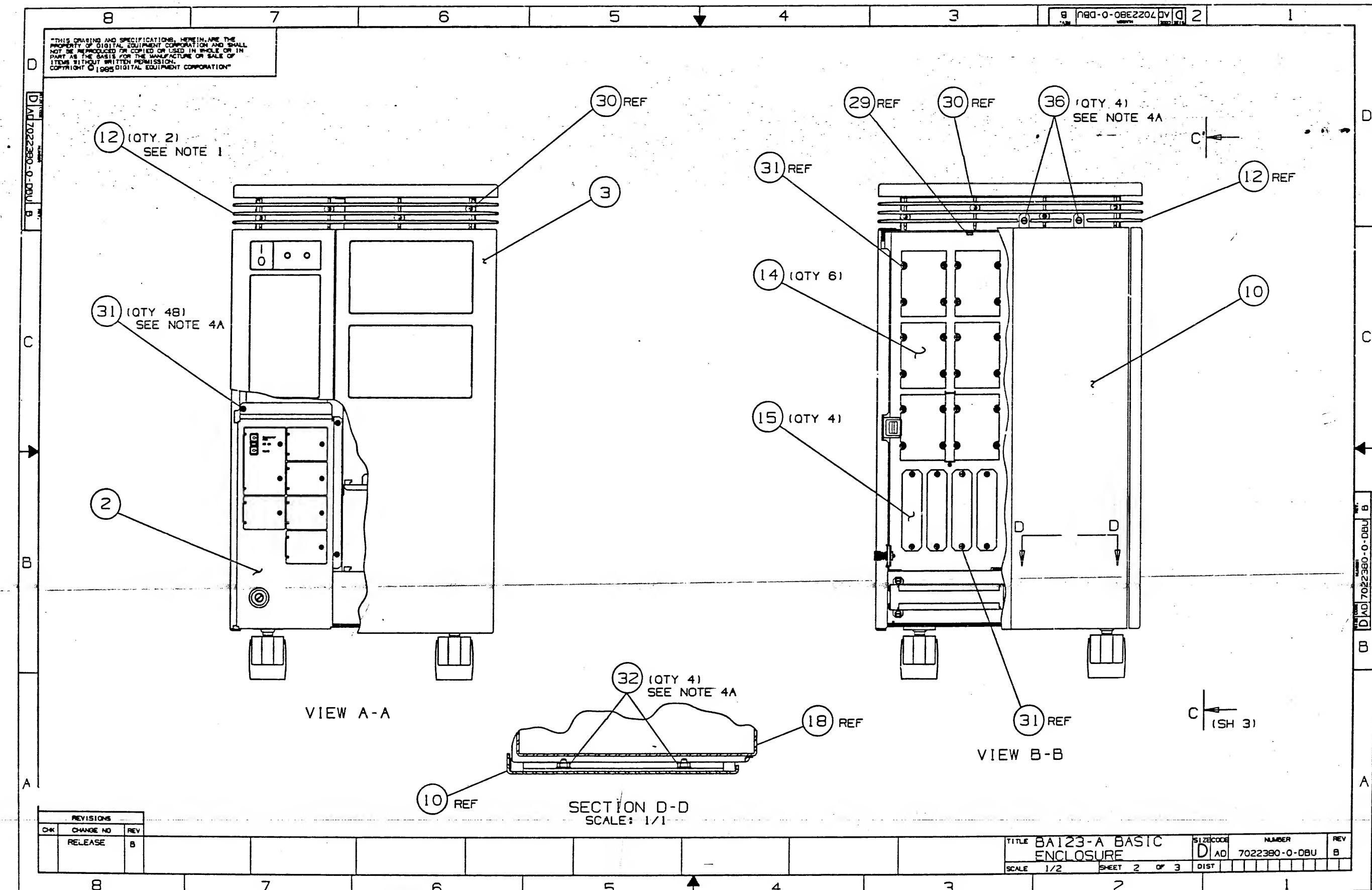
NOTES:

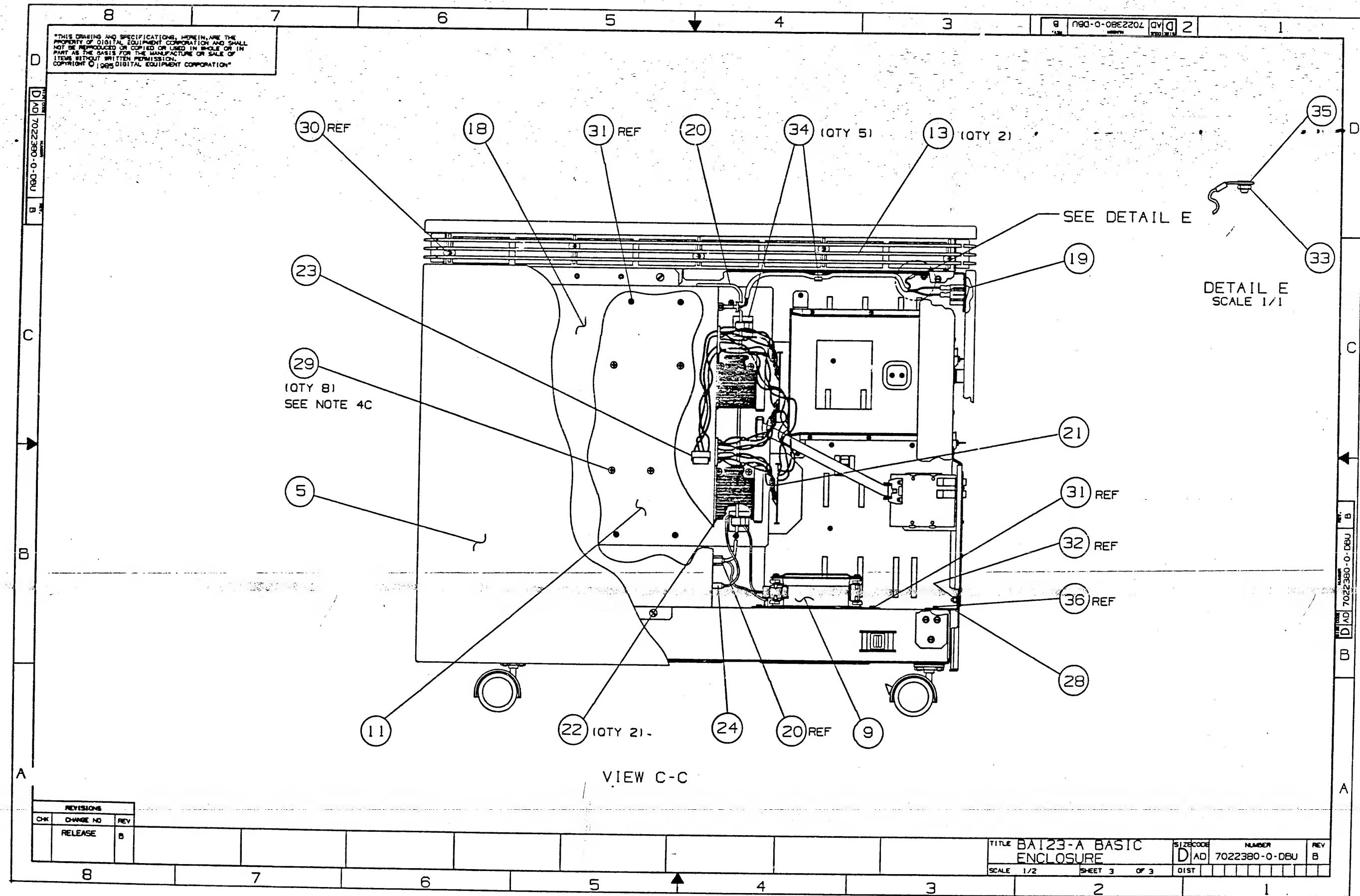
1. ITEM #12 (LOUVE, SHORT) TO BE ORIENTATED BY ITS MARKING LOCATED ON THAT ITEM.
2. ITEMS #34 (CABLE CLAMP) TO BE LOCATED APPROX WHERE SHOWN.
3. LOCATE ITEMS 27, 41, 42 OR 43, 44 OR 45 APPROX WHERE SHOWN NEAR SIDE.
4. TORQUE REQUIREMENTS ARE AS FOLLOWS:
 - A. ITEMS #31, 32 & 36 SHALL BE 8 TO 11 INCH-LBS
 - B. ITEM #30 TO BE 6 TO 8 INCH-LBS
 - C. ITEM #29 TO BE 18 TO 24 INCH-LBS.
5. WORKMANSHIP TO BE PER DEC STD 187

VIEW E-E

CAUTION: OFF SHEET PARTS LIST EXISTS
REFER TO K-PL-7022380-0-DBP
(ML 752)

		DESCRIPTION	DRAWING NO.	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)					
INCHES TOLERANCES		ANGLES 60° & 30°	SURFACE QUALITY	DIMENSION RANGE IN INCHES	
QUANTITY & VARIATION	INCHES	DEGREES	MICRINCHES	OVER .000	OVER .000
	.000 ± .002	.000 ± .002		.000	.000
	.000 ± .005	.000 ± .005		.012	.012
	.000 ± .008	.000 ± .008		.018	.018
	.000 ± .010	.000 ± .010		.024	.024
	.000 ± .015	.000 ± .015		.036	.036
THIRD ANGLE PROJECTION					
DO NOT SCALE DRAWING					
REMOVE BURRS AND BREAK SHARP CORNERS					
MATERIAL SEE PARTS LIST					
FINISH NONE					
		ON D. PELLEGRINO	DATE 17-DEC-84	TITLE digital	
		CHG'D J. KUSHAGIN	DATE 14-FEB-85		
		DES. DS. J. KWONG	DATE 17-DEC-84		
		REP. DS. J. KWONG	DATE 17-DEC-84		
		MFG. DS. J. EDWARDS	DATE 17-DEC-84		
		TOP DEC. D-AD-7022380-0-DBU	REV. B	DOCUMENT NUMBER	
		SIZE CODE NUMBER D AD 7022380-0-DBU B			
		SCALE 1/2 SHEET 1 OF 3			





LINE ITEM TOP DOCUMENT

PART NUMBER REV DESCRIPTION

VARIATION REVISION LEVEL:

QTY PER VARIATION	
01	02
A1	A1

1	1	D-AD-7021991-0-DBU	7021991-01	FRAME ASSEMBLY	1	1
2	2	C-AD-7021996-0-DBU	7021996-01	CONTROL PANEL ASSY.	1	1
3	3	D-AD-7021997-0-DBU	7021997-01	PANEL COVER FRONT DISK ASSY	1	1
4	4	D-AD-7021999-0-DBU	7021999-01	TOP COVER ASSY.	1	1
5	5	D-AD-7022000-0-DBU	7022000-01	SIDE PANEL ASSY L/H	1	1
6	6	D-AD-7022001-0-DBU	7022001-01	SIDE PANEL ASSY R/H	1	1
7	7	D-AD-7022003-0-DBU	7022003-01	FAN MOUNT CARD CAGE ASSY.	1	1
8	8	D-IA-7022006-0-DBU	7022006-01	COVER FRONT CARD CAGE ASSY.	1	1
9	9	D-AD-7022296-0-DBU	7022296-01	FAN MOUNT MASS STORAGE ASSY	1	1
10	10	D-AD-7022339-0-DBU	7022339-01	DOOR, REAR ASSY.	1	1
11	11	D-IA-7430692-0-DBU	7430692-01	COVER, REAR, CARD CAGE	1	1
12	12	D-MD-7430709-0-DBU	7430709-01	LOUVRE, SHORT	2	2
13	13	D-MD-7430710-0-DBU	7430710-01	LOUVRE, LONG	2	2
14	14	C-IA-7427574-0-0	7427574-01	PLATE, COVER	6	6
15	15	B-MD-7428683-0-DBU	7428683-01	PLATE, CONNECTOR BLANK	4	4
16	16	E-UA-5417507-0-DBU	5417507-01	QBUS BACKPLANE, 13 SLOTS, QUAD	1	1
17	17	D-UA-5416665-0-DBU	5416665-01	REMOTE SENSE OF TEMPERATURE FOR	1	1
18	18	D-PS-3023616-0-DBU	3023616-01	P.S. 460W 2DC REGULATOR BDS, FAN	1	1
19	19	A-PS-1700859-0-0	1700859-01	CABLE ASSY, AC, ON/OFF POWER	1	1
20	20	A-PS-1700863-0-0	1700863-01	CABLE ASSY, FAN	1	1
21	21	A-PS-1700870-0-0	1700870-01	CABLE ASSY, DC POWER DRIVE	1	1
22	22	A-PS-1700865-0-0	1700865-01	CABLE ASSY, 18COND	2	2
23	23	A-PS-1700911-0-0	1700911-01	CABLE ASSY, 9POS POWER DRIVE	1	1
24	24	A-PS-1700864-0-0	1700864-01	CABLE ASSY, FAN	1	1
25	25	A-PA-3700821-0-0	3700821-01	PKG COMPUTER, BA123 CUSTOMER	1	1
26	26	A-PS-3624253-0-0	3624253-01	LABEL, I/O, BULKHEAD	1	1
27	27	A-PS-3624254-0-0	3624254-01	LABEL, MU BUSINESS COMPUTER	1	1
28	28	C-MD-7431225-0-DBU	7431225-01	BRACKET, CONTROL PANEL	1	1
29	29		9010174-01	SCREW, SEMS PAN PHIL	8-	8
30	30		9000055-01	SCREW, THD RL, PAN POZI F/METL	4	18

REVISION HISTORY

BASIC PART NO: 7022380

ENG	ECO NUMBER	REV	SECTION A OF A	DRN:	S. STEFANICK	DATE: 18-DEC-84	D	I	G	I	T	A	L
INITIAL	B		SECTION VARIATION INDEX [A]01,02	CHK'D:	J. KUSHAGIN	DATE: 13-FEB-85	TITLE PARTS LIST BA123-A BASIC ENCLOSURE						
			[B]	DES.ENG:	J. KWONG	DATE: 18-DEC-84	DOCUMENT NUMBER						
			[C]	RESP.ENG.:	J. KWONG	DATE: 18-DEC-84	SIZE	CODE	NUMBER		REV		
			[D]	MFG.ENG.:	J. EDWARDS	DATE: 18-DEC-84	K	PL	7022380-0-DBP		B		
			[E]	ASSEMBLY NUMBER:		RELEASE DATE: 06-MAR-85							
			[F]	B-DD-7022380-0-DBU	TOP DOCUMENT NUMBER: B-DD-7022380-0-DBU	FILE NAME: ML752B.PLS						EDIT #	23

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LINE ITEM TOP DOCUMENT

MIN	PART NUMBER	REV	DESCRIPTION	VARIATION REVISION LEVEL:		QTY	PER VARIATION
				01	02		
31	31		9009701-00 SCREW,SEMS PAN PHIL	6-	48	48	
32	32		9006560-00 NUT,HEX EXT TOOTH LCKWSHR	6-32	4	4	
33	33		9007651-00 WASHER,LOCK EXTERNAL STEEL		1	1	
34	34		9010016-00 CLAMP, CABLE, ADH BACK		5	5	
35	35		9006565-00 NUT,HEX EXT TOOTH LCKWSHR	10-32	1	1	
36	36		9010075-03 SCREW,TAP HEXWW THD RL	6-	4	4	
37	37		9907588-01 ENVELOPE,CLEAR ADH BACK		1	1	
38	38	D-AR-7022380-0-DBU	BA123-A SYSTEM ARRANGEMENT		REF	REF	
39	39	K-SP-BA123-A-DBF	ENG. SPEC BA123-A		REF	REF	
40	40		1700083-00 PWR CORD,TERM 3-14 SJT	125	1	-	
41	41		3615087-04 LABEL,"DANGER-HIGH CURRENT"		1	1	
42	42		3617905-16 LABEL,WARNING EQUIP. RATING,100-		1	-	
43	43		3617905-17 LABEL,WARNING EQUIP. RATING,220-		-	1	
44	44	A-PS-3624471-0-0	3624471-01 LABEL,BUSINESS COMP BA123-A2		1	-	
45	45	A-PS-3624471-0-0	3624471-02 LABEL,BUSINESS COMP BA123-A3		-	1	

46 NOTE: ITEMS #25 AND #40 NOT SHOWN ON FIELD OF DWG.

!TITLE	!SECTION A OF A	!SIZE	!CODE	DOCUMENT NUMBER	!REV
D I G I T A L	BA123-A BASIC ENCLOSURE	K	PL	7022380-0-DBP	B

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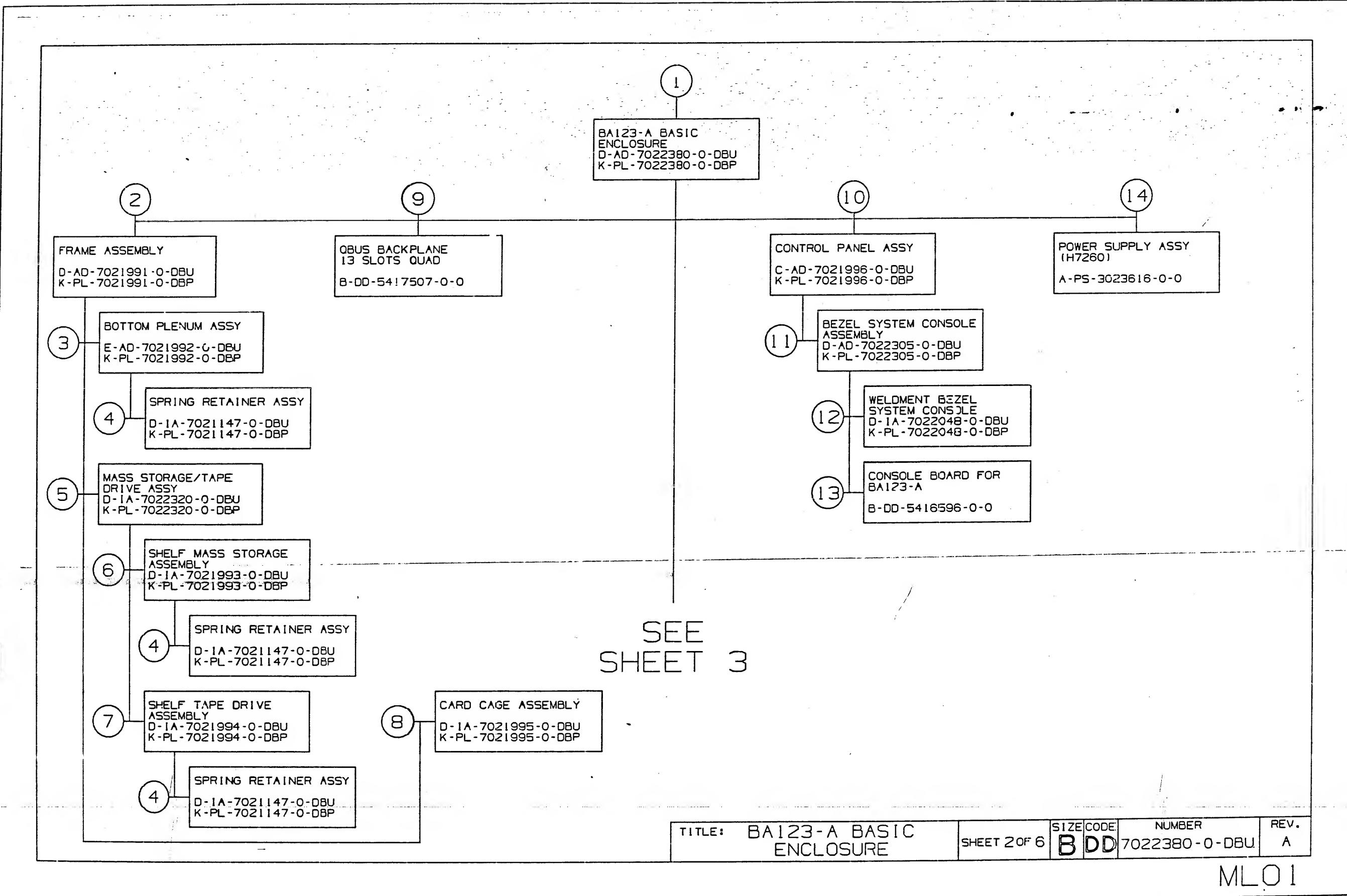
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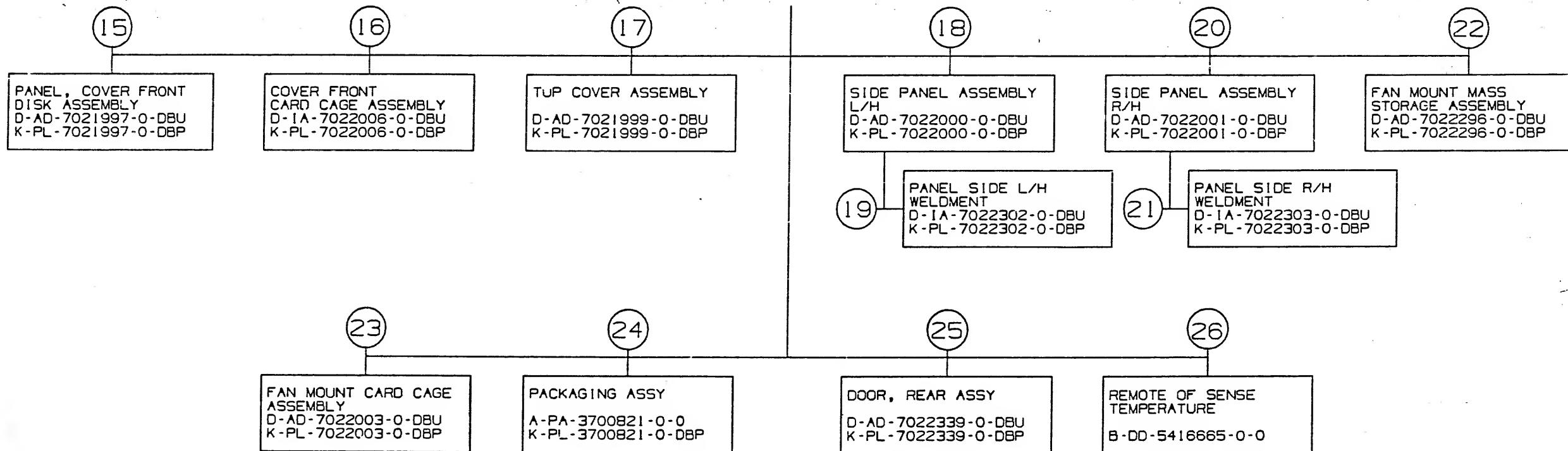
UNIT VARIATIONS

FILE NAME: DD7022380 - O - DBUA

ML01



CONT FROM
SHEET 2



TITLE:	BA123-A BASIC ENCLOSURE	SHEET 3 OF 6	SIZE CODE	NUMBER	REV.
			B DD	7022380-0-DBU	A

ML01

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

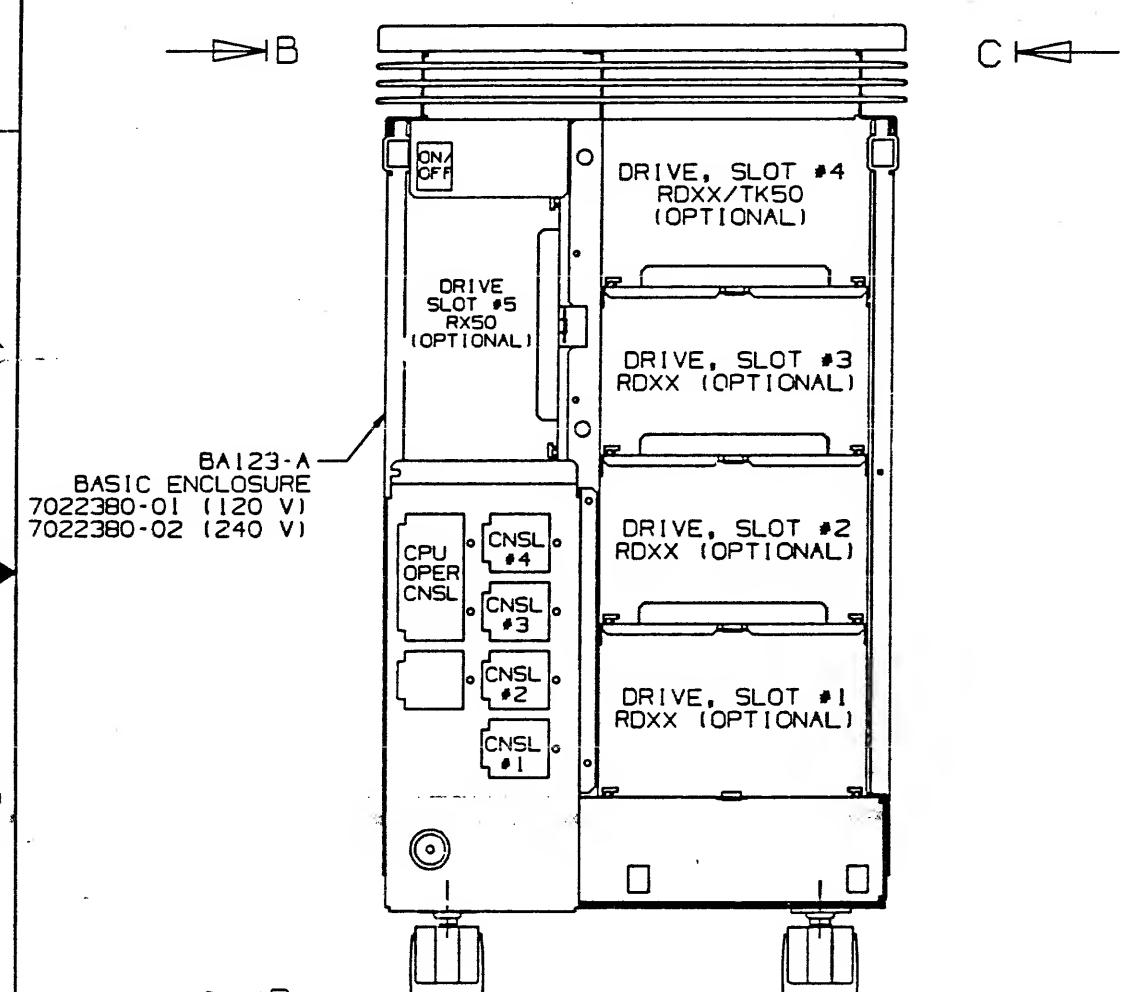
TITLE: BA123-A BASIC
ENCLOSURE

SHEET 4 OF 6 SIZE CODE NUMBER REV.
B DD 7022380-0-DBU A

ML01

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE	FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
					A-SS-7022048-0-1	SILK SCREEN	M
7	D-IA-7021994-0-DBU	SHELF TAPE DRIVE ASSEMBLY	M	13	B-DD-5416596-0-0	CONSOLE BOARD FOR BA123-A	E/M
	K-PL-7021994-0-DBP	SHELF TAPE DRIVE ASSEMBLY (PL)	M				
	D-MD-7430746-0-DBU	SHELF TAPE DRIVE	M				
	D-MD-7427554-0-DBU	HALF SLIDE	M				
8	D-IA-7021995-0-DBU	CARD CAGE ASSEMBLY	M	14	A-PS-3023616-0-0	POWER SUPPLY ASSEMBLY (H7260)	E/M
	K-PL-7021995-0-DBP	CARD CAGE ASSEMBLY (PL)	M				
	E-IA-7430690-0-DBU	FRAME CARD CAGE	M				
	K-PL-7430690-0-DBU	FRAME CARD CAGE (PL)	M	15	D-AD-7021997-0-DBU	PANEL COVER FRONT DISK ASSY	M
	D-MD-7429632-0-DBU	CARD GUIDE 12 SLOT	M		K-PL-7021997-0-DBP	PANEL COVER FRONT DISK ASSY (PL)	M
	D-IA-7430693-0-DBU	BAFFLE, FCC	M		E-MD-7430704-0-DBJ	PANEL, FRONT	M
	K-PL-7430693-0-DBP	BAFFLE, FCC (PL)	M		C-MD-7431191-0-DBU	BRACKET, STUD	M
					E-MD-7430708-0-DBU	DOOR, FRONT	M
					C-MD-7431178-0-DBU	BRACKET, DOOR HINGE	M
					D-MD-7431477-0-DBU	PANEL, FILLER	M
9	B-DD-5417507-0-0	OBUS BACKPLANE 13 SLOTS QUAD	E/M				
10	C-AD-7021996-0-DBU	CONTROL PANEL ASSEMBLY	M	16	D-IA-7022006-0-DBU	CARD CAGE FRONT COVER ASSY	M
	K-PL-7021996-0-DBP	CONTROL PANEL ASSEMBLY (PL)	M		K-PL-7022006-0-DBP	CARD CAGE FRONT COVER ASSY (PL)	M
	E-IA-7430705-0-DBU	PANEL CONTROL	M		E-IA-7430691-0-DBU	COVER FRONT CARD CAGE	M
	K-PL-7420705-0-DBP	PANEL CONTROL (PL)	M		K-PL-7430691-0-DBP	COVER FRONT CARD CAGE (PL)	M
	C-MD-7431171-0-DBU	BEZEL, BLANK	M		D-MD-7430828-0-DBU	SUPPORT MODULES	M
					D-MD-7431479-0-DBU	SUPPORT, MODULE REMOVEABLE	M
11	D-AD-7022305-0-DBU	BEZEL, SYSTEM CONSOLE ASSY	E/M	17	D-AD-7021999-0-DBU	TOP COVER ASSEMBLY	M
	K-PL-7022305-0-DBP	BEZEL, SYSTEM CONSOLE ASSY (PL)	E/M		K-PL-7021999-0-DBP	TOP COVER ASSEMBLY (PL)	M
	A-PS-1700860-0-0	CABLE ASSY, CONSOLE BACKPLANE	E/M		D-IA-7430707-0-DBU	COVER, TOP	M
					K-PL-7420707-0-DBP	COVER, TOP (PL)	M
					C-MD-7423357-0-DBU	KEY BUTTON	M
					D-IA-7431045-0-DBU	BRACKET, COVER	M
					K-PL-7431045-0-DBP	BRACKET, COVER (PL)	M
12	D-IA-7022048-0-DBU	WELDMENT, BEZEL SYS CONSOLE	M				
	K-PL-7022048-0-DBP	WELDMENT, BEZEL SYS CONSOLE (PL)	M				
	D-MD-7431169-0-DBU	BRACKET, SUPPORT SYSTEM CONSOLE	M				
	D-MD-7431173-0-DBU	BEZEL, SYSTEM CONSOLE	M	18	D-AD-7022000-0-DBU	SIDE PANEL ASSEMBLY L/H	M
					K-PL-7022000-0-DBP	SIDE PANEL ASSEMBLY L/H (PL)	M
TYPE: E ELECTRICAL M MECHANICAL E/M ELECTRO/MECHANICAL	digital			TITLE: BA123-A BASIC ENCLOSURE	SIZE CODE	NUMBER	REV.
	digital				SHEET 5 OF 6	B DD	7022380-0-DBU A

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE	FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
				25	D-AD-7022339-0-DBU	DOOR, REAR ASSY	M
					K-PL-7022339-0-DBP	DOOR, REAR ASSY (PL)	M
					E-IA-7431043-0-DBU	DOOR, REAR	M
					K-PL-7431043-0-DBP	DOOR, REAR (PL)	M
19	D-IA-7022302-0-DBU	PANEL, SIDE L/H WELDMENT	M		E-IA-7430703-0-DBU	PANEL, REAR	M
	K-PL-7022302-0-DBP	PANEL, SIDE L/H WELDMENT (PL)	M		K-PL-7430703-0-DBP	PANEL, REAR (PL)	M
	E-MD-7431042-0-DBU	PANEL, LEFT	M		D-MD-7431188-0-DBU	HINGE, REAR DOOR LINING	M
	B-MD-7431190-0-DBU	BRACKET STUD SIDE PANEL	M				
20	D-AD-7022001-0-DBU	SIDE PANEL ASSEMBLY R/H	M	26	B-DD-5416665-0-0	REMOTE OF SENSE TEMPERATURE	E/M
	K-PL-7022001-0-DBP	SIDE PANEL ASSEMBLY R/H (PL)	M				
21	D-IA-7022303-0-DBU	PANEL, SIDE R/H WELDMENT	M				
	K-PL-7022303-0-DBP	PANEL, SIDE R/H WELDMENT (PL)	M				
	D-MD-7430702-0-DBU	PANEL SIDE	M				
	B-MD-7431190-0-0	BRACKET, STUD SIDE PANEL	M				
22	D-AD-7022296-0-DBU	FAN MOUNT MASS STORAGE ASSY	M				
	K-PL-7022296-0-DBP	FAN MOUNT MASS STORAGE ASSY (PL)	M				
	D-MD-7430711-0-DBU	BRACKET, FAN MOUNT MASS STORAGE	M				
23	D-AD-7022003-0-DBU	FAN MOUNT CARD CAGE ASSY	M				
	K-PL-7022003-0-DBP	FAN MOUNT CARD CAGE ASSY (PL)	M				
	D-MD-7430694-0-DBU	BRACKET, FAN MOUNT CARD CAGE	M				
24	A-PA-3700821-0-0	PACKAGING ASSY	M				
	K-PL-3700821-0-DBP	PACKAGING ASSY (PL)	M				
TYPE: E ELECTRICAL M MECHANICAL E/M ELECTRO/MECHANICAL				TITLE: BA123-A BASIC ENCLOSURE		SIZE CODE SHEET 6 OF 6 B DD	NUMBER 7022380-0-DBU A REV. ML01
DRB 108A				digital			

8	7	6	5	↓	4	↑	3	↓	2	↑	1
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 <p>The diagram shows the internal configuration of the BA123-A basic enclosure. It features five drive slots labeled #1 through #5. Drive #1 is an RDX (optional). Drives #2, #3, and #4 are RDXX (optional), while drive #5 is RX50 (optional). A power supply unit is located at the bottom. On the left side, there is a control panel with an 'ON/OFF' switch and several 'CNSL' buttons numbered #1 through #4. External ports include two serial ports (COM1 and COM2) and a power input port.</p>											

NOTES:

1. RDX SIGNAL DISTRIBUTION (M9058) IS SHOWN FOR REF ONLY AND NOT PART OF BA123-A. (SEE SHEET 5).
2. FOR REAR PANEL RULES AND CONFIGURATION SEE SHEET 3.
3. FOR POWER HARNESS WIRING DIAGRAM SEE SHEET 6.
4. FOR MODULE RULES SEE SHEET 6.
5. MASS STORAGE CONFIGURATION RULES:
THE POWER SUPPLY IN THE BA123-A ENCLOSURE CAN POWER UP TO FOUR OF THE FIVE DRIVE SLOTS ONLY.
THE FOLLOWING ARE SOME OF THE COMBINATIONS:
 - (4) RD52'S
 - RX50, TK50, (2) RD52'S
 - TK50, (3) RD52'S

FILE NAME: AR7022380-0-DBUA

PLOT AT .5000

FIRST HIGHER ASSEMBLY D-AD-BA123-A-DBP		QUANTITY & VARIATION	DESCRIPTION	DRAWING NO.	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 1141)						
THICKNESS TOLERANCES	ANGLES TOLERANCES	APP. FORM & POSITION TOLERANCES	DIMENSION RANGE IN INCHES			
.001 ± .002	.001 ± .002	.001 ± .002	OVER 0.000	OVER 0.000	OVER 0.000	OVER 0.000
.001 ± .002	.001 ± .002	.001 ± .002	OVER 0.000	OVER 0.000	OVER 0.000	OVER 0.000
.001 ± .002	.001 ± .002	.001 ± .002	OVER 0.000	OVER 0.000	OVER 0.000	OVER 0.000
WORKHOLDERS						
DO NOT SCALE DRAWING						
REMOVE BURRS AND BREAK SHARP CORNERS						
MATERIAL	FINISH	TOP SURF.	DATE	DATE	DATE	DATE
//	//	D-AR-7022380-0-DBU	08-JAN-85	08-MAR-85	08-MAR-85	08-MAR-85
J. KWONG	J. EDWARDS	08-MAR-85	08-MAR-85	08-MAR-85	08-MAR-85	08-MAR-85
TITLE: BA123-A SYSTEM ARRANGEMENT						
DOCUMENT NUMBER: D-AR 7022380-0-DBU A						
REV. A	REV. B	REV. C	REV. D	REV. E	REV. F	REV. G
INITIAL						

VIEW A-A
(SEE SHEET 2)
SHOWN WITHOUT FRONT
OR SIDE PANELS

REVISIONS
CHANGE NO.
INITIAL

8

7

6

5

4

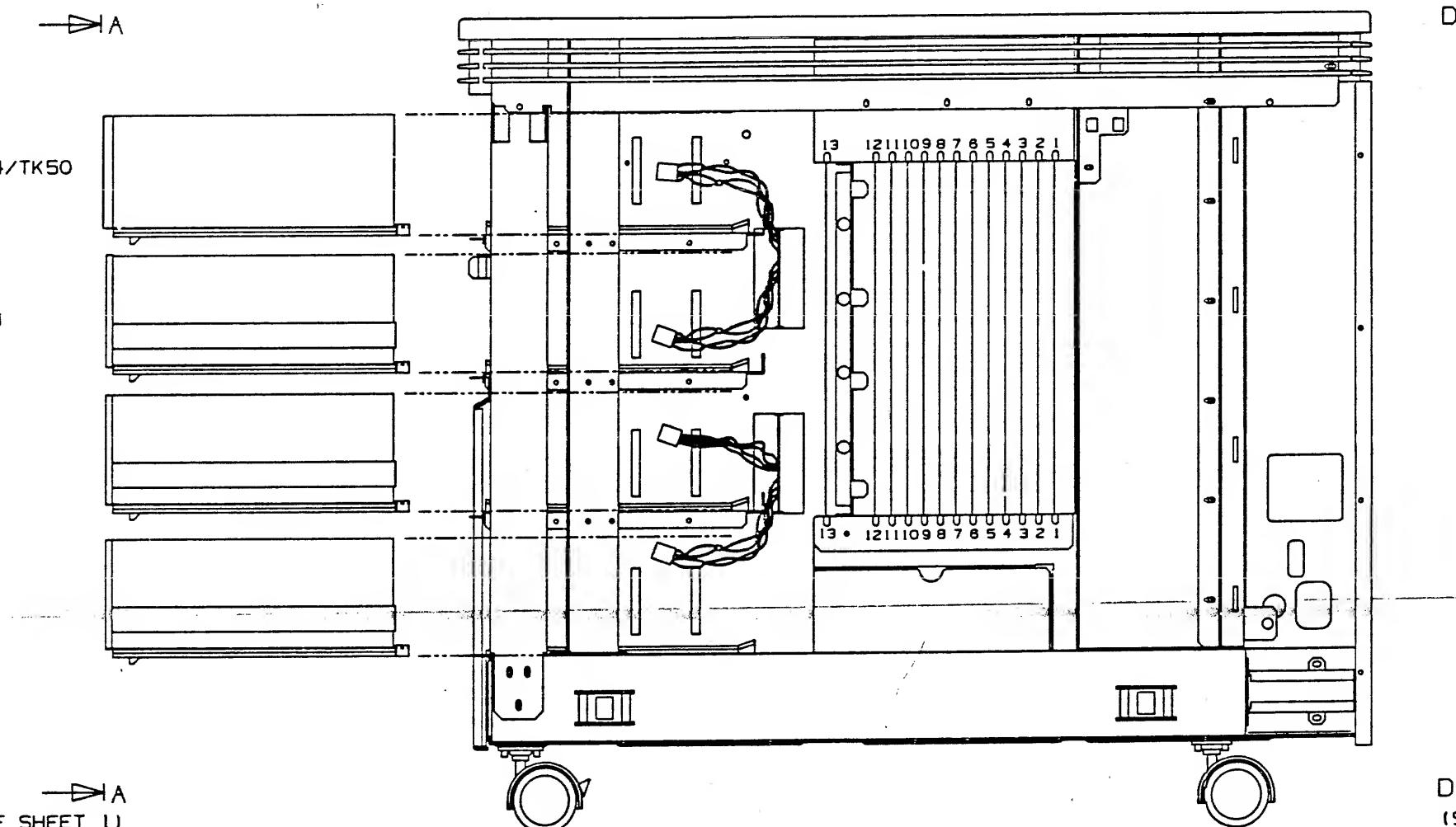
3

2

1

ML01

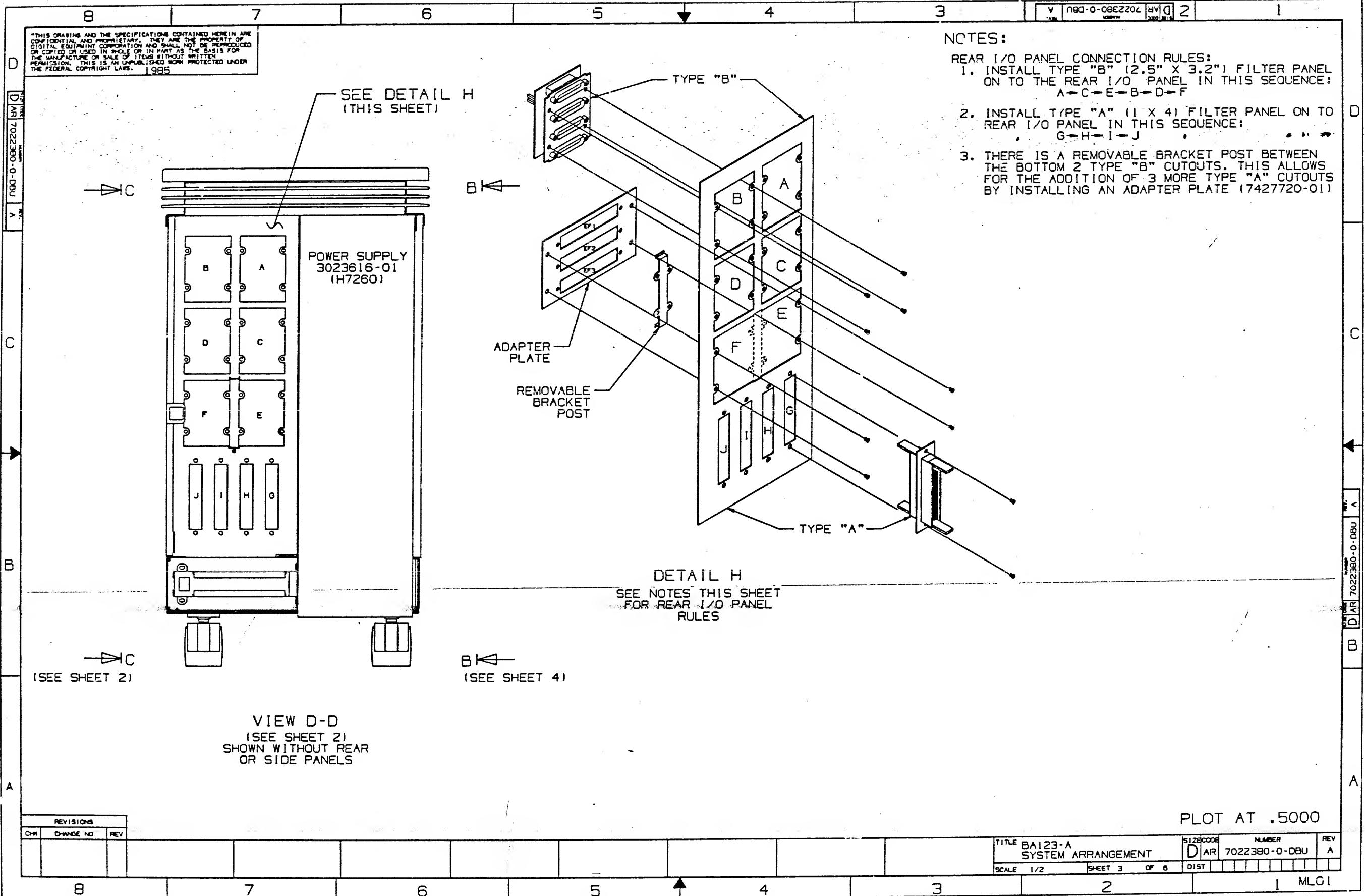
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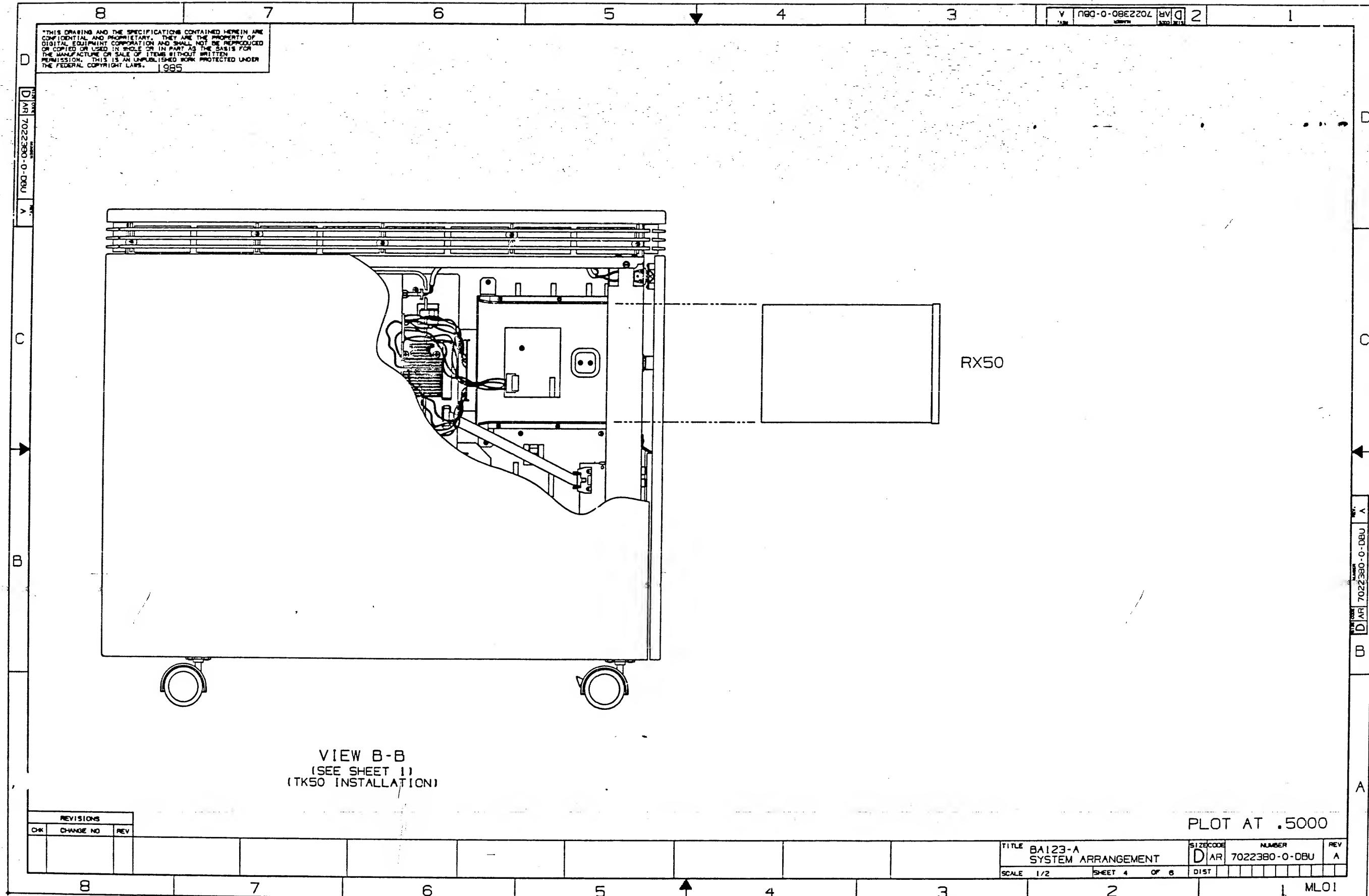


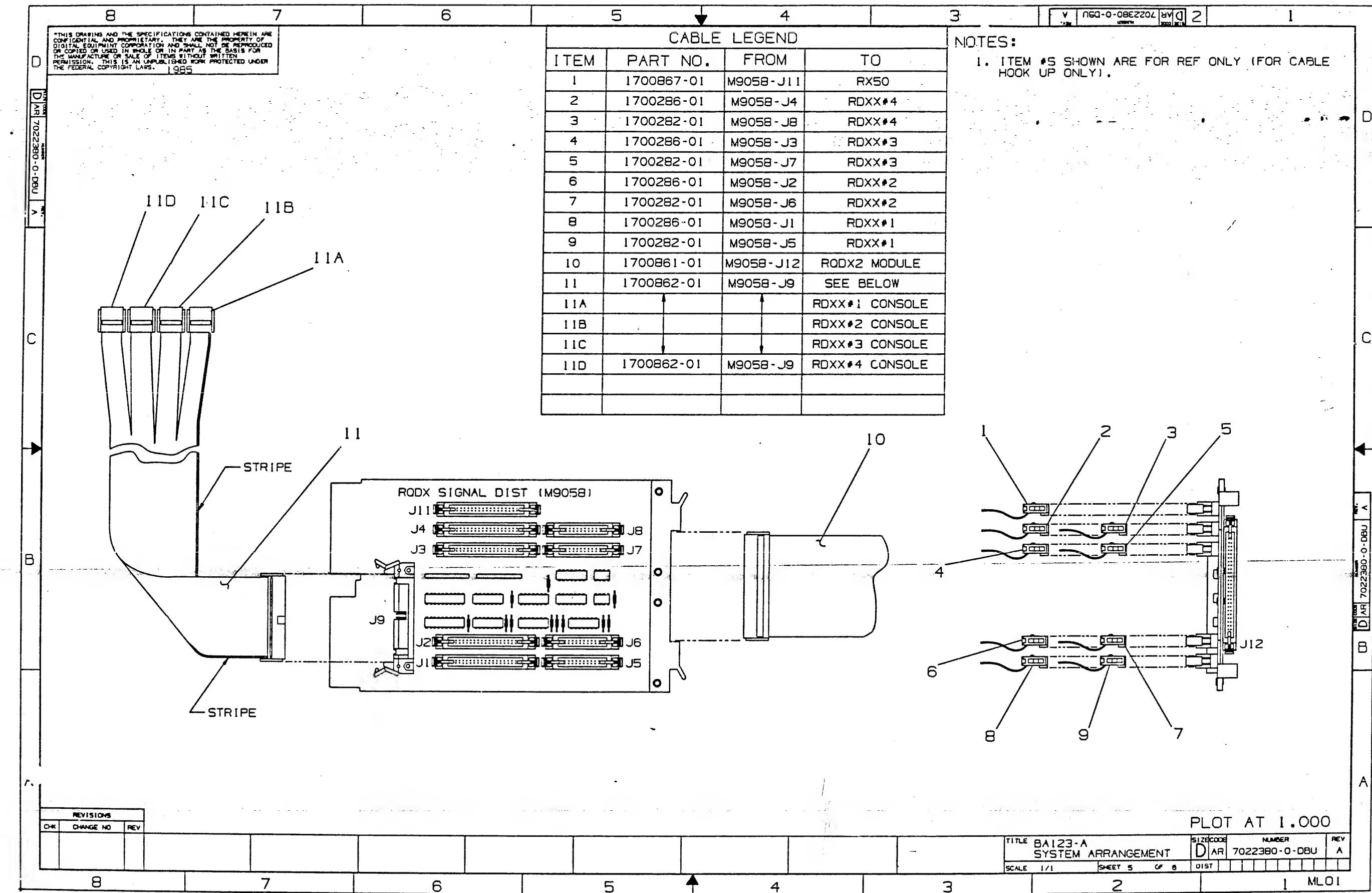
VIEW C-C
(SEE SHEET 1)
SHOWN WITHOUT FRONT
OR REAR PANELS

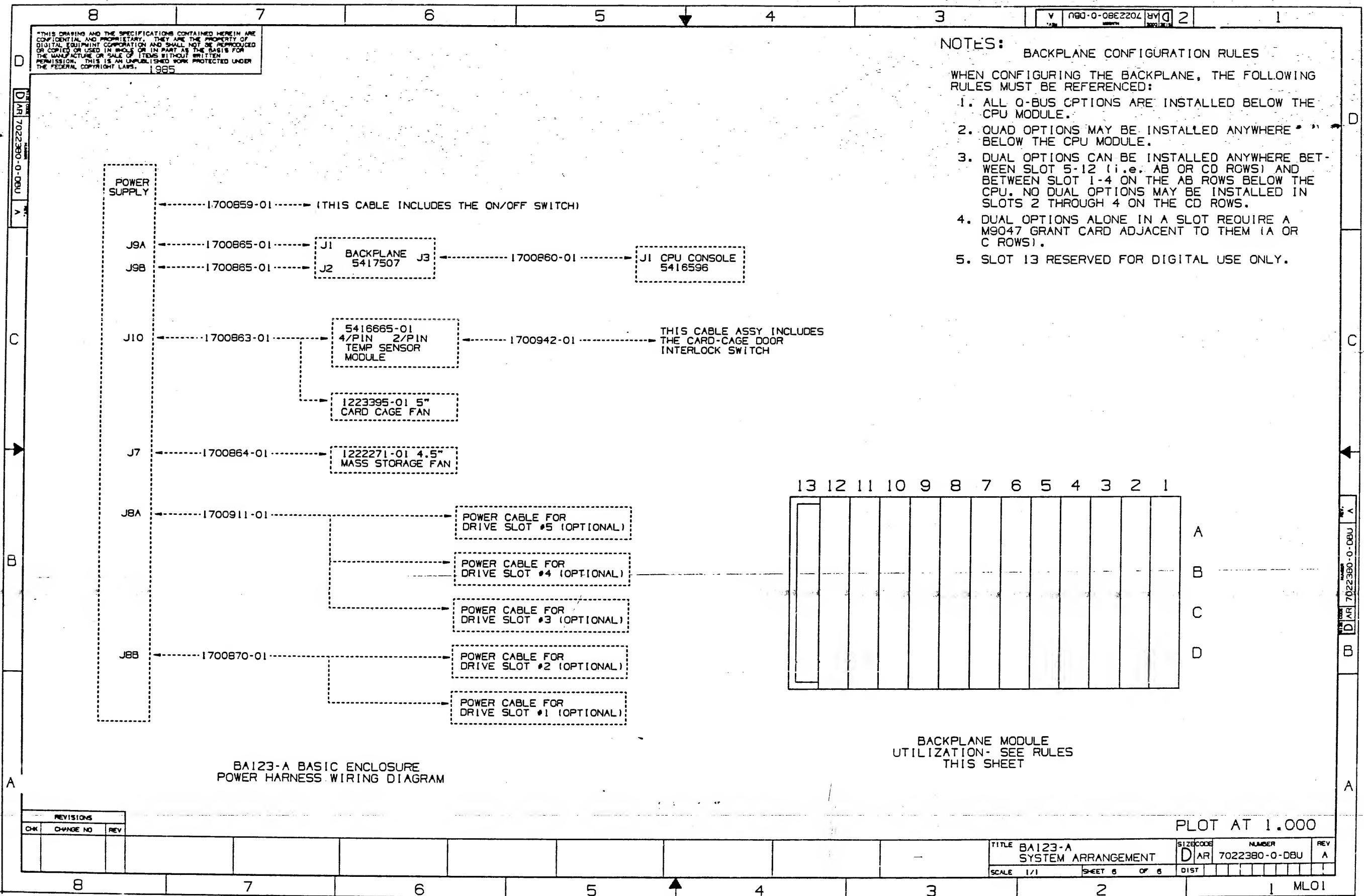
PLOT AT .5000

SIZE	CODE	NUMBER	REV
D	AR	7022380-0-DBU	A
6	DIST		
			1. MLOI









A standard linear barcode representing the document number 5H17507-0-0.

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USED ON OPTION/MODEL	DRN.	S. MARIE	DATE	26 SEP 84	TITLE	BACKPLANE		
	CHK'D	<i>Marie</i>	DATE	9-25-84		BA123-A		
	DES. ENG.	<i>Marie</i>	DATE	26 SEP 84	DOCUMENT NUMBER			
	RESP. ENG.	<i>Marie</i>	DATE	26 SEP 84	SIZE	CODE	NUMBER	REV.
	MFG. ENG.	R. BELIVEAU	DATE	3/1/85	B	DD	5417507-0-0	A
		R. BELIVEAU		3/1/85			SHEET 1 OF 1	

LINE ITEM TOP DOCUMENT

MIN

PART NUMBER REV DESCRIPTION

QTY PER VARIATION

01

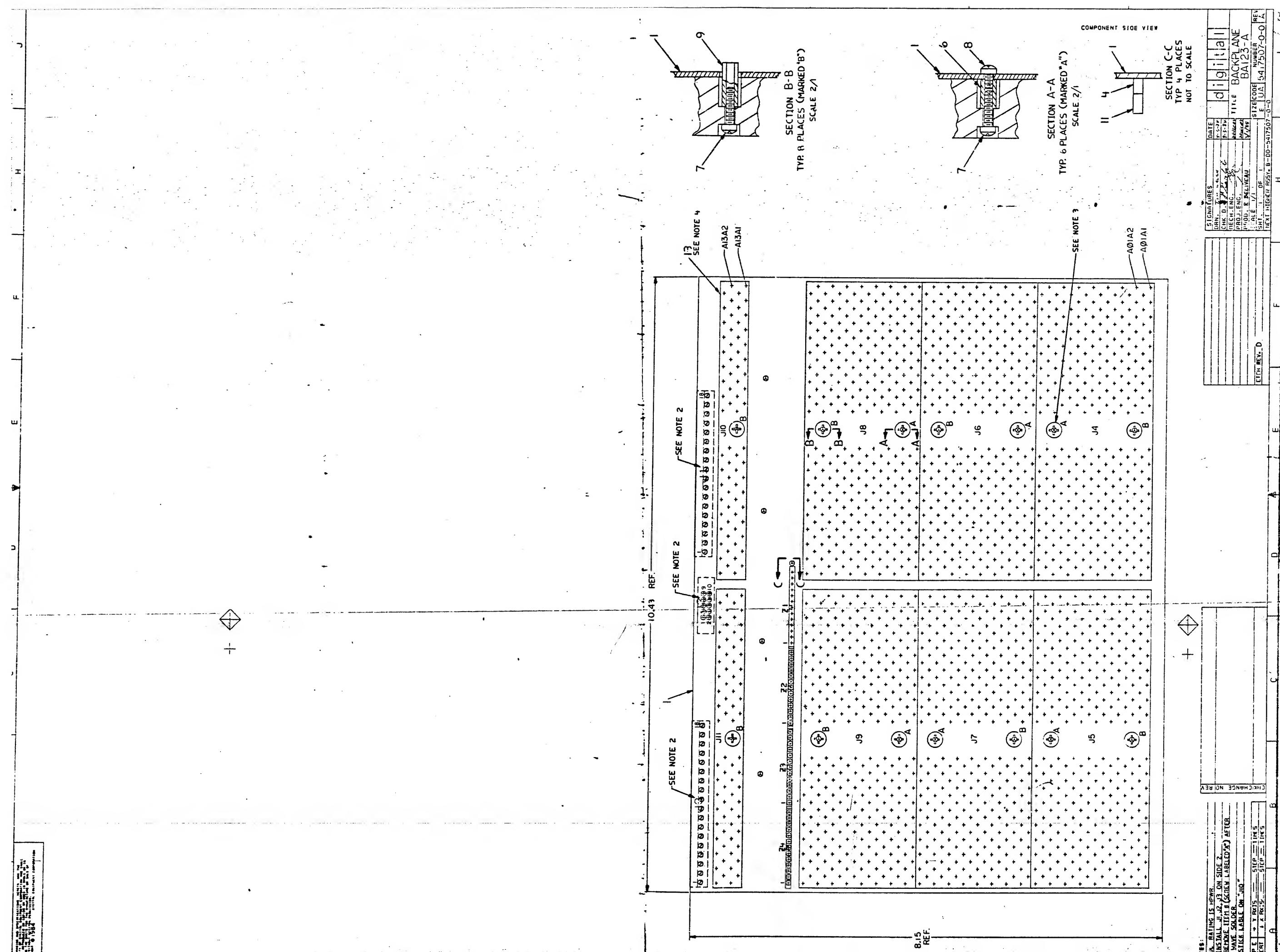
REFERENCE DESIGNATOR

VARIATION REVISION LEVEL: A1

1	1	D-MD-5017506-0-0	5017506-01	ETCHED BOARD	1	
2	2		1214886-05	PCB HEADER 10POS(2X 5).100CC	1	J2
3	3		1215699-07	PCB, HEADER 18POS(1X18).156CC STR	2	J1, J3
4	4		1217535-05	SKT, IC 13PIN SIP TIN SOLD	4	XZ1-XZ4
5	5		7417041-00	288 PIN CONNECTOR	6	J4-J9
6	6		9000033-12	SPACER, THREADED HEX ALUM 8-3	6	
7	7		9006120-06	SCREW, FILL POZI 8-	14	
8	8		9006035-01	SCREW, MACH PAN PHIL 8-	6	
9	9		9009246-00	SPACER, THREADED HEX ALUM 8-3	8	
10	10		7411881-01	DECAL	1	
11	11		1323505-01	R NETWORK 180/390 2.0 % 13PIN	4	Z1-Z4
12	12		7417042-00	72 PIN CONNECTOR	2	J10-J11
13	13		3623593-01	LABEL, BLANK, PAPER, PIN FEED	1	
14	14		9905016-03	CARTON, DIE CUT, SELF LOCK W/FOAM	1	

REVISION HISTORY			BASIC PART NO: 5417507	DRN:	S. MANSOR	DATE: 07-JUN-84	D	I	G	T	A	L
ENG	ECO NUMBER	REV	SECTION A OF A	CHK'D:	F. GAROFALO	DATE: 1-MAR-85	TITLE		PARTS LIST			
	INITIAL	A	SECTION VARIATION INDEX	DES.ENG:	T. ORR	DATE: 1-MAR-85	13 SLOT BACKPLANE					
			[A] 01						DOCUMENT NUMBER			
			[B]						SIZE	CODE	NUMBER	REV
			[C]									
			[D]									
			[E]									
			[F]									
			[G]									
			[H]									
			[I]									
			[J]									
			[K]									
			[L]									
			[M]									
			[N]									
				ASSEMBLY NUMBER:			TOP DOCUMENT NUMBER:		FILE NAME:		EDIT #	
				E-UA-5417507-0-0			B-DD-5417507-0-0		TW261A.PLS			4

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SIZE	CODE	5416596-0-0	REV.	B
------	------	-------------	------	---

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION			REVISIONS												
		5416596-01	BA123-A FRONT PANEL			A1	A2											
D-UA-5416596-0-0	1		BA123-A FRONT PANEL			A	A											
D-CS-5416596-0-1	1		BA123-A FRONT PANEL			A	A											
K-PL-5416596-0-DBP	1		BA123-A FRONT PANEL			A	B											
K-PC-5416596-0-DBC			P.C. DESIGN DATA BASE			A	A											
		5016595-01	ETCHED CIRCUIT BOARD			B1	B1											
B-DD-5016595-0-0	1		DRAWING DIRECTORY			A	A											
K-SP-5416596-0-DBF	6		BA123-A FRONT PANEL			A	A											
NOTES:																		
REVISION HISTORY				DATE	ECO NO.	REV.												
6-84 INIT					A													
5-85 ML001					B													
								DRN.	B. LENNON	DATE	27JUN84	TITLE						
								CHK'D	R. BARRIERE	DATE	27JUN84	BA123-A FRONT PANEL						
								DES. ENG.	J. PADGETT	DATE	27JUN84	DOCUMENT NUMBER						
								RESP. ENG.	J. PADGETT	DATE	27JUN84	NUMBER						
								MFG. ENG.	R. BELLIVEAU	DATE	27JUN84	5416596-0-0						
								REV.				B						
								SHEET	1	OF	1							

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LINE ITEM	TOP DOCUMENT	PART NUMBER	REV	DESCRIPTION	MIN	VARIATION REVISION LEVEL:	QTY PER VARIATION	REFERENCE DESIGNATOR	
								01	A2
1	1	D-MD-5016595-0-0	5016595-01	CIRCUIT DRILL AND ETCH			1		
2	2		1000021-00	220.0 MMF 100V 5%200PPM MICA	1		1	C1	
3	3		1005636-00	22 MFD .6V 10% S.TANT	1		1	C2	
4	4		1012784-00	.047 MFD .50V +80-20% CER	2		2	C3,C4	
5	5		1012312-01	.47 MFD .50V +80-20% CER	1		1	C5	
6	6		1017472-00	10 MFD .35V +75-10% AL EL	1		1	C6	
7	7		1100114-00	PIV=.25 I0=135 MA			1	D1	
8	8		1119827-01	LED, SUPERBRIGHT, RED T1 PKG			1	D2	
9	9		1116622-02	LED 2.0MCD@25M			1	D3	
10	10		1121248-01	GREEN LED T1 4MCD 1"LEADS			1	D4	
11	11		1110864-00	LED 2MCD@10MA			2	D5,D6	
12	12		1218945-03	SW,PB,LT 1PST NO-MOMENTARY .25A			1	S1	
13	13		1218945-01	SW,PB,LT 1PST NO-MAINTAIN .25A			1	S2	
14	14		1217310-07	SW,DIP 2POS/1PST 5VDC100MA S			1	S3	
15	15		1216832-07	*** THIS ITEM IS NOT USED ***			1		
16	16		1219918-01	SKT,SWITCH 4PIN RT ANGLE			2	XS1,XS2	
17	17		1300250-00	150.0 .25 W 5.0 % CF			1	R1	
18	18		1311523-00	110.0 .25 W 5.0 % CF			1	R2	
19	19		1300271-00	220.0 .25 W 5.0 % CF			1	R3	
20	20		1302388-00	2.0 K .25 W 5.0 % CF			4	R4,R5,R6,R7	
21	21		1300479-00	10.0 K .25 W 5.0 % CF			4	R10-R13	
22	22		1302514-00	39.0 K .25 W 5.0 % CF			2	R14,R15	
23	23		1302466-00	100.0 K .25 W 5.0 % CF			1	R16	
24	24		1300391-00	1.50 K .25 W 5.0 % CF			2	R8,R9	
25	25		1914987-00	8641-2 TRANSCEIVER,UNIBUS,QU			1	E1	
26	26		1912858-00	LS221 ONE SHOT-DUAL,SCHMIT			1	E2	
27	27		1914156-01	LM 393AN VOLT COMPARATOR,DUA			1	E3	
28	28	D-MD-7430089-0-DBU	7430089-01	HOLDER,L.E.D.,SINGLE			1		
29	29		1209941-05	PCB,HEADER 10PIN(2X10).100CC 90D			1	J1	
30	30		1209941-04	PCB,HEADER LATCH			1		

REVISION HISTORY		BASIC PART NO: 5416596		DRN:	M. FUNARO	DATE: 16-MAR-84	D	I	G	I	T	A	L
ENG	ECO NUMBER	REV	SECTION A - OF A	CHK'D:	D. BARRIERE	DATE: 16-MAR-84	TITLE: PARTS LIST BA123-A FRONT PANEL						
JP	INITIAL	A	SECTION VARIATION INDEX	DES.ENG:	J. PADGETT	DATE: 16-MAR-84	DOCUMENT NUMBER						
JP	5416596-ML001	B	[A] 01 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]	RESP.ENG.:	J. PADGETT	DATE: 16-MAR-84	SIZE	CODE	NUMBER	! REV			
				MFG.ENG.:	R. BELIVEAU	DATE: 18-MAY-84	K	PL	5416596-0-DBP	B			
				ASSEMBLY NUMBER:		TOP DOCUMENT NUMBER:		FILE NAME:	EDIT #				
				D-UA-5416596-0-0		B-DD-5416596-0-0		Z9241B.PLS	15				

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LINE ITEM TOP DOCUMENT

MIN

QTY PER VARIATION

01

REFERENCE DESIGNATOR

PART NUMBER REV DESCRIPTION

VARIATION REVISION LEVEL: A2

31 31

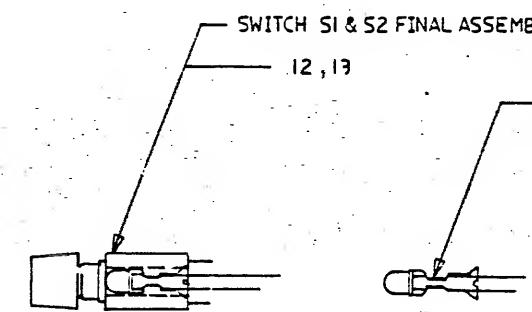
1209941-03

PCB, HEADER LATCH

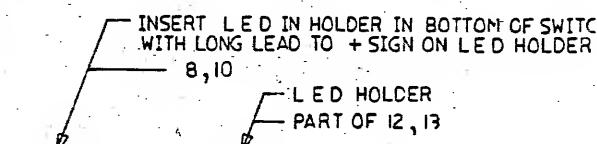
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DIGITAL		TITLE	SECTION A OF A		SIZE	CODE	DOCUMENT NUMBER	REV
D	I	BA123-A FRONT PANEL	K	PL	5416596-0-DBP	B		

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CRIMP LEADS



INSERT LED IN HOLDER IN BOTTOM OF SWITCH
WITH LONG LEAD TO + SIGN ON LED HOLDER

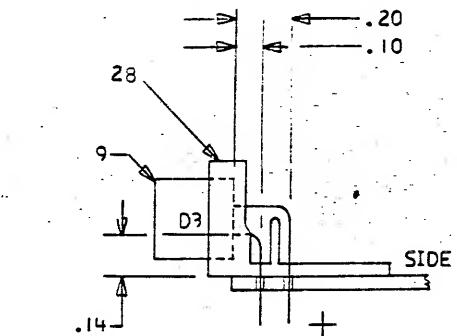
LED HOLDER
PART OF 12, 13

DETAIL A

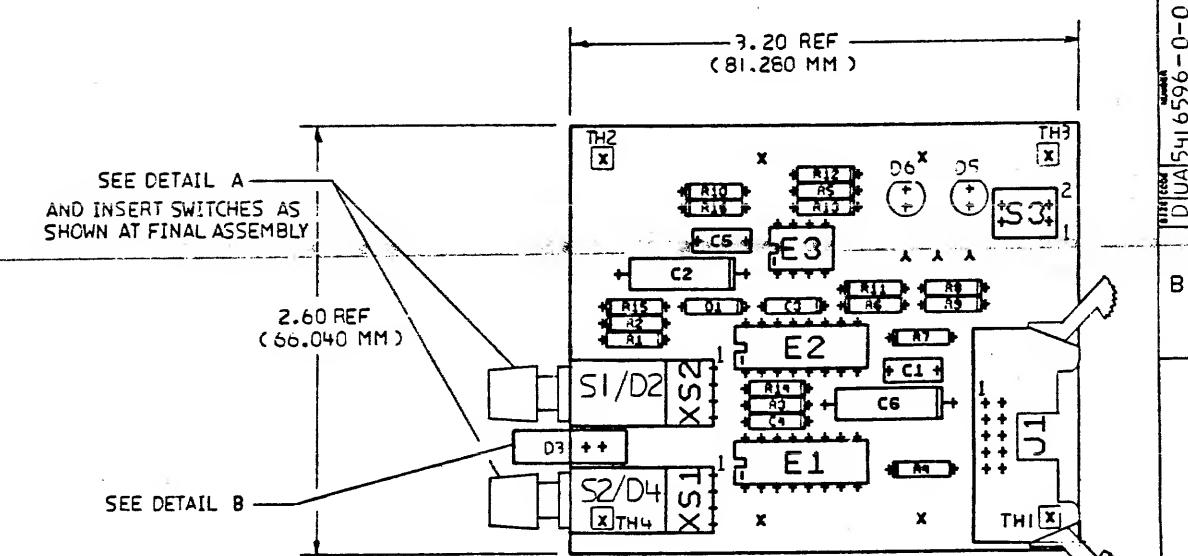
NOT TO SCALE

AFTER PLACING LED ASSY IN
SWITCH ASSY AS SHOWN TURN
CLOCKWISE 1/4 TURN

REF S1, S2



DETAIL B
NOT TO SCALE



8

A

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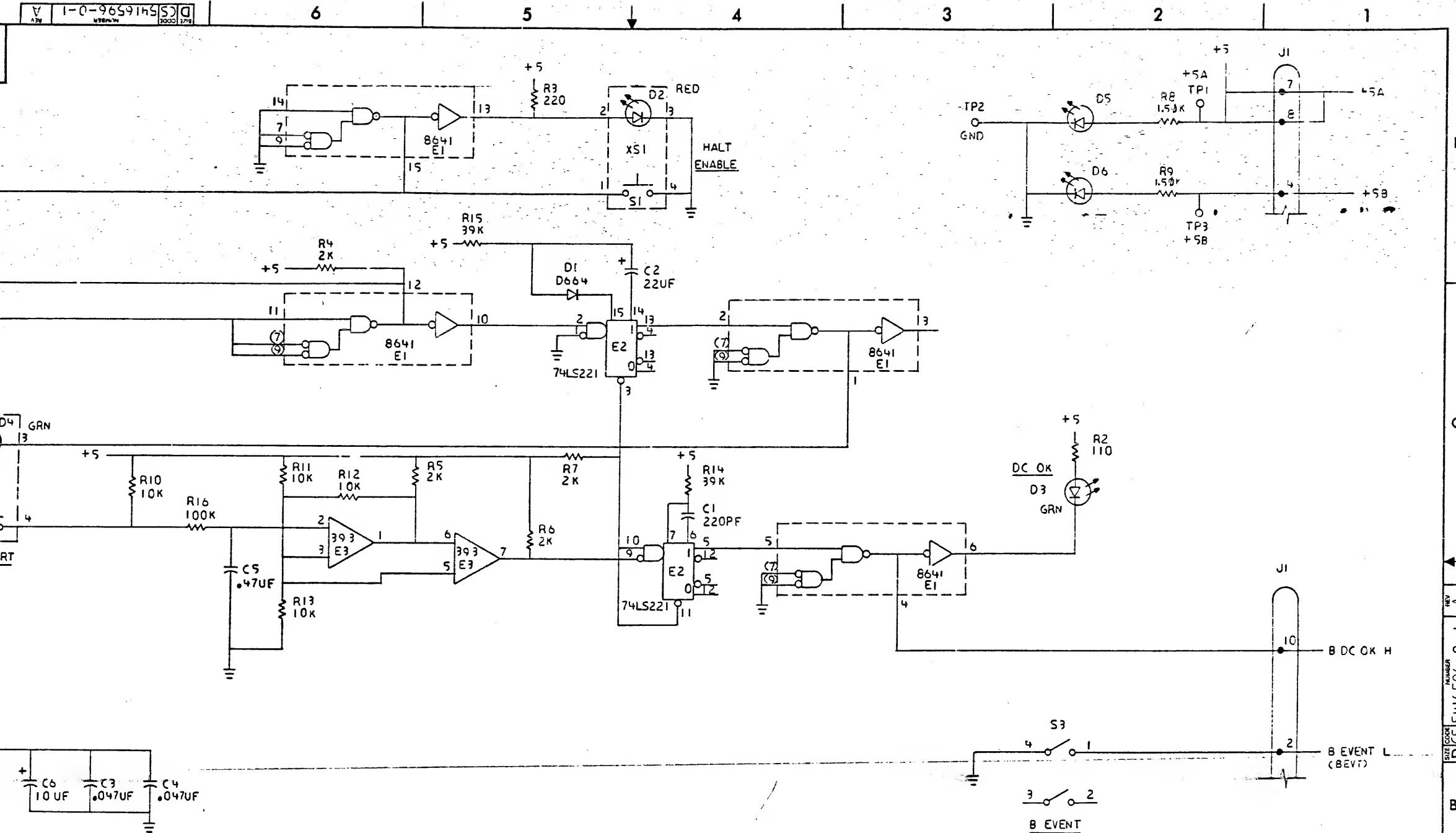
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REVISION HISTORY	REV

8

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1

DRW: B. S. Angale	DATE: 2-3-84	TITLE: digital
CHG'D: L. L. Smith	DATE: 2-3-84	
DES ENG: James P. Smith	DATE: 2-3-84	
REP ENG: James P. Smith	DATE: 2-3-84	
MAN ENG: James P. Smith	DATE: 2-3-84	
NETW ENGINEER: B. S. Angale	DATE: 2-3-84	
DOCUMENT NUMBER: DCS 5416596-0-1		

BA123-A
FRONT PANEL

SIZE CODE: DCS 5416596-0-1 REV: A

C

B

A

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DRAWING DIRECTOR

ITEM	DRAWING NO.	NO. OF SHTS	PART NO.	DESCRIPTION	TYPE	REVISIONS						
						A1	A1	A2	B1	B1	B1	A
1			5416665-01	TEMP SENSOR BD.								
2	D-UA-5416665-0-0	1		TEMP SENSOR BD.		A	B	C				
3	D-CS-5416665-0-1	1		TEMP SENSOR BD.		A	A	A				
4	K-PL-5416665-0-DBP	1		TEMP SENSOR BD.		A	A	B				
5	K-PC-5416665-0-DBC			P.C. DESIGN DATA BASE		A	A	A				
6			5016664-01	ETCHED CIRCUIT BOARD		B1	B1	B1				
7	B-DD-5016664-0-0	1		DRAWING DIRECTORY		A	A	A				
NOTES:						DD REV	A	B	C			
REVISION HISTORY			CONT. REVISION HISTORY			MADE BY: P. LENNON DATE: 23-OCT-84						d i g i t a l
ENG	ECO NUMBER	REV	ENG	ECO NUMBER	REV	CHECKED BY: D. BARRIERE DATE: 23-OCT-84						TITLE DRAWING DIRECTORY
TO RL	INITIAL 5416665-ML001 5416665-MK002	A B C				DESIGN ENGINEER: T. ORR DATE: 23-OCT-84						TEMP SENSOR BD.
						RESPONSIBLE ENG: R. LIGENZA DATE: 04-FEB-86						
						PRODUCTION ENG: NEMI HARRIS DATE: 04-FEB-86						SIZE K CODE DD DOCUMENT NUMBER K-DD-5416665-0 REV. C

AUTOMATED BY VAXKPL (V1.0)

P A R T S L I S

LINE ITEM	TOP DOCUMENT	PART NUMBER	REV	MIN	MAX	QTY PER VAR/REV	SHEET A1 OF A
							REFERENCE DESIGNATORS
1	1	D-MD-5016654-0-0		50-16654-01	CIRCUIT DRILL & ETCH	1	
2	2			13-24146-01	*** THIS ITEM IS NOT USED ***	1	
3	3			12-23681-03	THERMOSTAT, NO C9 50C	1	
4	4			12-11342-04	MATE-N-LOK 04PIN(1X04).200CC HDR	1	TST
5	5			12-11342-02	MATE-N-LOK 02PIN(1X02).200CC HDR	1	J1
6	6			90-07254-00	TRANSIPADS #10146	1	J2
7	7		A	13-25634-01	A THERMISTOR, EPOXY COATED, 500OHM S	1	R1

SHEET A1 OF A1

REFERENCE DESIGNATORS

REVISION HISTORY

!KPL MODULE FORMAT!SECTION

A! DRN: T-03

P E S T I C I D E S

ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX	DATE: 25-OCT-84	D I G I T A L
TO : INITIAL		A	[A] 01	CHK'D: D. BARRIERE	TITLE PARTS LIST
RL : 5416665-MK002		B	[B]	DATE: 25-OCT-84	TEMP SENSOR BD
		C	[C]		
		D	[D]	DES.ENG: T. ORR	
		E	[E]	DATE: 25-OCT-84	
		F	[F]		DOCUMENT NUMBER
		G	[G]		SIZE CODE
		H	[H]		NUMBER
		I	[I]		REV
		J	[J]	RESP.ENG.: T. ORR	
		K	[K]	DATE: 25-OCT-84	K PL 5416665-0-DBP
		L	[L]	MFG.ENG: B. LAIDMAN	8
		M	[M]	DATE: 25-OCT-84	RELEASE DATE:
		N	[N]		RELEASE STATUS: UNDER CHANGE
		O	[O]		
		P	[P]		
		Q	[Q]		
		R	[R]		
		S	[S]		
		T	[T]		
		U	[U]		
		V	[V]		
		W	[W]		
		X	[X]		
		Y	[Y]		
		Z	[Z]		

BASIC PART NUMBER: D-UA-5416665-0-0 TOP DOCUMENT NUMBER: B-00-5416665-0-0 FILE NAME: MK1283.PLS EDIT # 2

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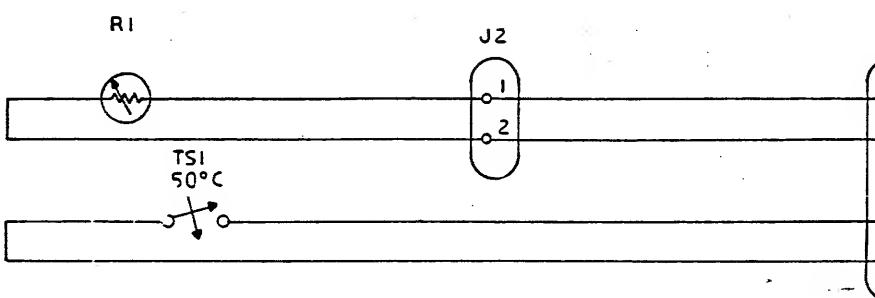
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DCS 5416665-0-1 A

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D

D

C

C

B

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A

REVISION HISTORY	ECO NUMBER	REV.
DATE		

8

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1

REV. S. DiAngelo	DATE 29 OCT 84	TITLE digital
CHG. R. Brune	DATE 24 OCT 84	
DEL. CHG. J. Pickett	DATE 13 OCT 84	
REP. CHG. J. Pickett	DATE 13 OCT 84	
APL. CHG. J. L. Lewis, PF	DATE 21 NOV 84	
NON-PRODUCTION TOP DOC NO. B-DD-5416665-0		DOCUMENT NUMBER DCS 5416665-0-1 A
SCALE 1:1 SHEET 01 OF 01		